IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

In re:	)
	)
	) MDL Docket No. 07-md-1848 (GMS)
REMBRANDT TECHNOLOGIES, LP	) CHIEF JUDGE GREGORY M. SLEET
PATENT LITIGATION	)
	)
	)

PARTIES' JOINT CLAIM CONSTRUCTION CHART (THE EIGHT PATENTS)

Attached hereto are the following:

Exhibit A contains the claims of the Eight Patents, marked to identify subparts of

the asserted claims as referenced in the parties' claim charts attached as Exhibits A and B.

Exhibit B is the parties' Joint Claim Construction Chart for "The Eight Patents"

without intrinsic evidence references.

Exhibit C is the parties' Joint Claim Construction Chart for "The Eight Patents"

with intrinsic evidence references.

<table>
<tr><td>

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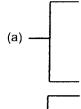</td><td>

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EXHIBIT A

ʾ631 Patent

5,852,631

(a)

1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of:

(b)

establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and

(c)

establishing said link layer connection based upon said negotiated physical layer modulation.

3. The method of claim 1, wherein said link layer connection is an error-correcting protocol.

4. The method of claim 1, further comprising the step of presetting link layer parameters of said link layer connection to default settings based on said negotiated physical layer modulation.

5. The method of claim 3, wherein said error-correcting protocol includes parameters that are set to pre-defined settings based on said negotiated physical layer modulation.

6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising:

means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and

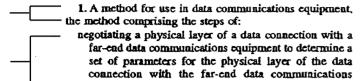means for establishing said link layer connection based upon said negotiated physical layer modulation.

8. The system of claim 6, wherein said link layer connection is an error-correcting protocol.

9. The system of claim 6, further comprising means for presetting link layer parameters of said link layer connection to pre-defined settings based on said negotiated physical layer modulation.

10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising:

logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and

logic for establishing link layer connection based upon said negotiated physical layer modulation.

'761 Patent

5,710,761

1. A method for use in data communications equipment, the method comprising the steps of:

negotiating a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the physical layer of the data connection with the far-end data communications equipment; and
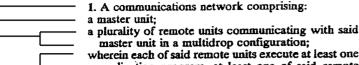
selecting one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

2. The method of claim 1, further including the step of

negotiating error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

3. The method of claim 1, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

6. The method of claim 1, wherein the at least one parameter is the data rate negotiated with the far-end data communications equipment.

9. Data communications apparatus comprising:

a memory that stores a number of error control negotiation sequences; and

processor circuitry that negotiates a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the physical layer of the data connection with the far-end data communications equipment, and then selects from memory one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

10. The apparatus of claim 9, wherein the processor negotiates error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

11. The apparatus of claim 9, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

14. The apparatus of claim 9, wherein the at least one parameter is data rate negotiated with the far-end data

'819 Patent

4,937,819

1. A communications network comprising:
a master unit;
a plurality of remote units communicating with said master unit in a multidrop configuration;
wherein each of said remote units execute at least one application program, at least one of said remote units executing at least two application programs, said remote units receiving messages outbound from said master unit and responding in a time slot assigned to each of said application programs;
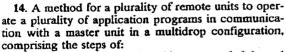said master unit including a master network timing means with a period which is divided into a plurality of subframes, wherein each subframe is divided into said time slots, and each of said time slots is used as an interval in which one of said application programs in said one of said remote units is assigned to transmit to said master unit in a time division multiple access fashion; and
said master unit including ranging means communicating with said master network timing means wherein a transmission time between said master unit and each of said respective remote units is calculated and transmitted from said master unit to each of said respective remote units, each of said respective remote units using said transmission time to adjust initiation of said time slots.

2. The network of claim 1 wherein said remote units include a reservation request generator which activates a reservation request bit for requesting an additional time interval inbound to said master unit, and wherein said master unit includes a reservation request processor communicating to said master network timing means, said reservation request processor being responsive to said reservation request bit.

11. The network of claim 2 wherein said time slot comprises a format so as to include a preamble, a poll response data bit, said reservation request bits, at least one priority bit and error detection bit.

12. The network of claim 1 wherein the master unit includes means for calculating clock drifts of the remote units and issuing reset commands to correct the same whereby each remote unit determines its transmit epoch accurately, thereby minimizing guard time while maintaining contention-free transmission to said master unit, said means for calculating clock drifts and issuing reset commands being in communication with said master network timing means.

14. A method for a plurality of remote units to operate a plurality of application programs in communication with a master unit in a multidrop configuration, comprising the steps of:
calculating and storing in said master unit inbound and outbound transmission times between the master unit and said remote units;
dividing a period of a clock in said master unit into a number of subframes, dividing each subframe into a number of slots, each corresponding to transmission times for one of said remote units, and assigning a slot to each of said application programs in said one of said remote units;
transmitting from said master unit to each of said respective remote units the transmission time between said master unit and said respective remote unit, each of said respective remote units using said transmission time to adjust initiation of said slots; and
transmitting data from each of said remote units to said master unit in a time division multiple access configuration wherein each application in each remote unit transmits during said assigned subframe.
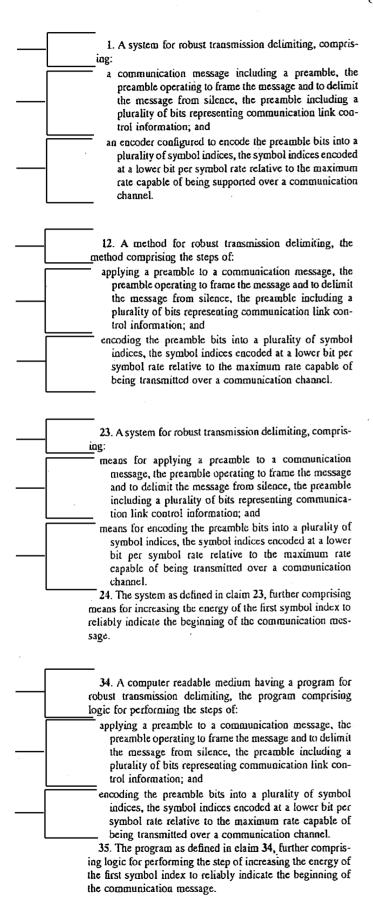
'858 Patent

5,719,858

1. Data communications apparatus comprising:

a time division multiplexed bus having a bandwidth, where a portion of the bandwidth is allotted to packet data;

a plurality of packet data sources coupled to the time-division multiplexed bus that share the allotted bandwidth for transmitting packet data; and

a distributed packet manager within each of said packet data sources configured to allocate access to the allotted bandwidth among said packet data sources.

7. Communications apparatus comprising:

a time-division multiplexed bus having a predefined bandwidth;

a plurality of synchronous data sources coupled to the time-division multiplexed bus for communicating synchronous data in a first portion of the predefined bandwidth;

a plurality of packet data sources coupled to the time-division multiplexed bus for communicating packet data in a second portion of the predefined bandwidth, where the plurality of packet data sources share the second portion of the predefined bandwidth for transmitting packet data; and

a distributed packet manager within each of said packet data sources configured to allocate access to the second portion of the predefined bandwidth among said packet data sources.

8. The apparatus of claim 7 further including a network access manager coupled to the time-division-multiplexed bus for communicating the synchronous data and the packet data to at least one network facility.

9. Communications apparatus comprising:

a time-division multiplexed bus having a predefined bandwidth;

a plurality of synchronous data sources coupled to the time-division multiplexed bus for communicating synchronous data in a first portion of the predefined bandwidth; and

a plurality of packet data sources coupled to the time-division multiplexed bus for communicating packet data in a second portion of the predefined bandwidth, where the plurality of packet data sources share the second portion of the predefined bandwidth for transmitting packet data, the second portion of the predefined bandwidth being shared in such a way that only one of the plurality of packet data sources accesses the second portion of the predefined bandwidth at a time.

10. The apparatus of claim 7 wherein each one of the plurality of packet data sources includes interface circuitry to the time-division multiplexed bus for synchronizing packet data to the time-division multiplexed bus.

11. Communications apparatus comprising:

a time-division multiplexed bus having a predefined bandwidth;

a plurality of synchronous data sources coupled to the time-division multiplexed bus for communicating synchronous data in a first portion of the predefined bandwidth;

a plurality of packet data sources coupled to the time-division multiplexed bus for communicating packet

15. A method for use in a data communications apparatus for transmitting packet data on a time-division multiplexed bus, the method comprising the steps of:

coupling a plurality of packet data sources to the time-division multiplexed bus;

allocating a portion of the bandwidth of the time-division multiplexed bus to the plurality of packet data sources in such a way that the allocated portion is shared among the plurality of packet data sources;

transmitting packet data from the plurality of packet data sources on the allocated portion of the bandwidth; and

controlling access by said packet data sources to the allocated portion of the bandwidth via a distributed packet manager within each of said packet data sources.

20. A method for transmitting packet data on a time-division multiplexed bus in data communications equipment, the method comprising the steps of:

allocating a portion of the bandwidth of the time-division multiplexed bus as a multiple-access packet channel;

coupling a plurality of packet data sources to the time-division multiplexed bus;

controlling the access by said packet data sources to the allocated portion of the bandwidth via a distributed packet manager within each of said packet data sources;

transmitting packet data from the one of the plurality of packet data sources having access to the multiple-access packet channel.

26. The method of claim 20 further comprising the step of coupling a network access module to the time-division multiplexed bus for receiving the packet data for transmission over a network facility.

'444 Patent

US 6,950,444 B1

1. A system for robust transmission delimiting, comprising:

    a communication message including a preamble, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

    an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel.

12. A method for robust transmission delimiting, the method comprising the steps of:

    applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

    encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

23. A system for robust transmission delimiting, comprising:

    means for applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

    means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

24. The system as defined in claim 23, further comprising means for increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

34. A computer readable medium having a program for robust transmission delimiting, the program comprising logic for performing the steps of:

    applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

    encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

35. The program as defined in claim 34, further comprising logic for performing the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

'903 Patent

5,008,903

1. An apparatus for calculating pre-emphasis coefficients for a transmitting modem in a communications system, including:

first transmitting means in the transmitting modem, including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency-dependent characteristics of an output of said first transmitting means;

receiving means for receiving said output from said first transmitting means;

generating means for generating parameters responsive to a noise spectrum of said output including means for calculating said noise spectrum of said output;

second transmitting means for transmitting said parameters to the transmitting modem, and

computing means for computing the pre-emphasis coefficients from said parameters.

2. The apparatus of claim 1 wherein said adjusting means includes a filter with several taps.

3. The apparatus of claim 2 wherein said filter includes at least nine taps.

4. The apparatus of claim 1 wherein said generating means includes a noise spectrum generator circuit.

5. The apparatus of claim 4 wherein said noise spectrum generator circuit includes:

determining means for determining best-fit transmitted data points from said output of said first transmitting means as received by said receiving means;

comparing means for determining a difference between said best-fit transmitted data points and said output as received by said receiving means thereby calculating said noise spectrum of said output.

6. An apparatus for calculating pre-emphasis coefficients for a transmitting modem in a communications systems, including:

first transmitting means in the transmitting modem, including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency-dependent characteristics of an output of said first transmitting means;

receiving means for receiving said output from said first transmitting means;

generating means, including a noise spectrum generator circuit, for generating parameters responsive to a noise spectrum of said output;

second transmitting means for transmitting said parameters to the transmitting modem; and

computing means for computing the pre-emphasis coefficients from said parameters;

wherein said noise spectrum generator circuit includes determining means for determining best-fit transmitted data points from said output of said first transmitting means as received by said receiving means; and comparing means for determining a difference between said best-fit transmitted data points and said output as received by said receiving means;

wherein said receiving means includes analog-to-digital conversion means and demodulating means which generates a complex signal; and wherein said noise spectrum generator circuit includes a phase corrector responsive to said complex signal; a slicer which determines, from said complex signal, best-fit transmitted data points from said first transmitted means; subtracting means for determining a difference between said best-fit transmitted data points and said complex signal; an inverse phase corrector responsive to said difference; and a complex discrete Fourier transform block responsive to said inverse phase corrector.

7. The apparatus of claim 6 wherein said phase corrector is responsive to equalization means and wherein said equalization means is responsive to said inverse phase corrector.

8. An apparatus for calculating pre-emphasis coefficients for a transmitting modem in a communications systems, including:

first transmitting means in the transmitting modem, including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency-dependent characteristics of an output of said first transmitting means;

receiving means for receiving said output from said first transmitting means;

generating means, including a noise spectrum generator circuit, for generating parameters responsive to a noise spectrum of said output;

second transmitting means for transmitting said parameters to the transmitting modem; and

computing means for computing the pre-emphasis coefficients from said parameters;

wherein said noise spectrum generator circuit includes determining means for determining best-fit transmitted data points from said output of said first transmitting means as received by said receiving means; and comparing means for determining a difference between said best-fit transmitted data points and said output as received by said receiving means; and

wherein said determining means includes eye pattern data.

15. The apparatus of claim 1 wherein said second transmitting means transmits over a secondary channel.

16. The apparatus of claim 15 wherein said secondary channel is a sideband of a channel of said first transmitting means.

17. The apparatus of claim 16 wherein said receiving means and said second transmitting means are incorporated into a single circuit.

18. The apparatus of claim 1 wherein said computing means converts said parameters from logarithmic to linear scale.

19. The apparatus of claim 1 wherein said computing means adjusts said parameters iteratively to adjust for resonator frequencies of said first transmitting means.

20. The apparatus of claim 1 wherein said computing means adjusts said parameters to assure a constant power output of said first transmitting means.

21. A method for calculating pre-emphasis coefficients for a transmitting modem in a communications systems, including the steps of:

transmitting from the transmitting modem;

adjusting frequency characteristics of output from said transmitting step responsive to the pre-emphasis coefficients;

receiving said output from said first transmitting means;

calculating a noise spectrum of said output;

generating parameters responsive to said noise spectrum of said output;

sending said parameters to the transmitting modem; and

computing the pre-emphasis coefficients from said parameters.

'159 Patent

6,131,159

1. A system comprising:

(a) a processor;

(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a type which may be completely updated in its entirety but which is not volatile, said memory being the only program memory in said system; and

(c) alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.

2. The system of claim 1 wherein said memory is an EEPROM memory.

3. The system of claim 1 wherein said memory consists of 2-FLASH EEPROM devices.

4. The system of claim 1 wherein said alterable storage means is an EEPROM memory.

5. The system of claim 1 further comprising translation means interposed between said alterable storage means and said memory, wherein said alterable storage means holds an address that translates between addresses directed to the memory via said translation means and addresses actually applied to the memory by said translation means.

6. A system comprising:

(a) a processor;

(b) a memory coupled to said processor, said memory being the only program memory in the system, said memory being completely updatable in its entirety b non-volatile, there being a set of programs stored said memory that are executed when the system nee to be initialized; and

(c) alterable memory means for storing a multi-l memory address that controls the starting addre accessed by the processor when initializing.

7. The system of claim 6 further comprising means l receiving a trigger signal at a telecommunications input port of the system to begin execution of said programs.

8. A system comprising;

(a) a processor;

(b) a memory and a communications port coupled to said processor, said communications port being adapted to communicate with devices which are external to said system, said memory being completely updatable in its entirety but non-volatile;

(c) a program module in said memory that, when activated by said processor, effects communication with said port; and

(d) operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port.

9. The system of claim 8 wherein:

(a) said memory contains a first set of programs and a second set of programs;

(b) said memory is at least twice the size of the size of the first set of programs; and

(c) said operationally alterable means sets the starting position of the program executed by said processor in connection with communication with said port at a second specified location that is M removed from the first location, M being half the size of said memory.

10. A system comprising:

(a) a processor;

(b) a communication port coupled to said processor, said communication port being adapted to communicate with devices which are external to said system;

(c) a memory coupled to said processor, said memory being non-volatile and capable of being completely updated in its entirety, said memory containing programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication through said communication port; and

(d) means for activating said program for controlling communication and receiving information through said communication port to modify the programs in said memory, said information including the program for controlling communication through said communication port and a command that is executed by said processor effectively when it is received.

11. The system of claim 10 wherein the communication port is a telecommunication port.

12. The system of claim 10 wherein the communication port is a telecommunication port and the programs execute the functions of a modem.

13. The system of claim 10 where the communication port receives commands to be executed by the processor and data to be stored in the memory.

14. The system of claim 10 wherein said means for receiving includes means for altering the program according to the information obtained by the means for receiving.

15. The system of claim 10 wherein said means for receiving modifies the programs by altering a portion of the memory contents pursuant to data received via said communication port.

16. The system of claim 10 wherein said means for receiving modifies the programs by replacing them with program data received via said communication port.

17. The system of claim 10 where the means for altering alters all of the programs in the system in a single communication session with said communication port.

18. A system comprising:

(a) a processor;

(b) a memory coupled to said processor, said memory being of a type, which is completely updatable in its entirety but non-volatile;

(c) a set of program means stored in said memory that are activated when said system needs to be updated wit a new set of programs, and

(d) alterable storage means for holding an offset memory address that is used to point to a starting address accessed by said processor when initializing.

19. The system of claim 18 wherein said memory is an EEPROM memory.

20. The system of claim 18 wherein said memory consists of 2 FLASH EEPROM devices.

21. The system of claim 18 wherein said alterable storage means is an EEPROM memory.

'234 Patent

5,778,234

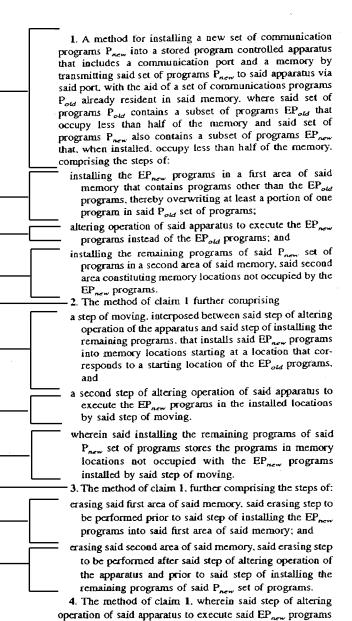1. A method for installing a new set of communication programs P_{new} into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs P_{new} to said apparatus via said port, with the aid of a set of communications programs P_{old} already resident in said memory, where said set of programs P_{old} contains a subset of programs EP_{old} that occupy less than half of the memory and said set of programs P_{new} also contains a subset of programs EP_{new} that, when installed, occupy less than half of the memory, comprising the steps of:

installing the EP_{new} programs in a first area of said memory that contains programs other than the EP_{old} programs, thereby overwriting at least a portion of one program in said P_{old} set of programs;

altering operation of said apparatus to execute the EP_{new} programs instead of the EP_{old} programs; and

installing the remaining programs of said P_{new} set of programs in a second area of said memory, said second area constituting memory locations not occupied by the EP_{new} programs.

2. The method of claim 1 further comprising

a step of moving, interposed between said step of altering operation of the apparatus and said step of installing the remaining programs, that installs said EP_{new} programs into memory locations starting at a location that corresponds to a starting location of the EP_{old} programs, and

a second step of altering operation of said apparatus to execute the EP_{new} programs in the installed locations by said step of moving.

wherein said installing the remaining programs of said P_{new} set of programs stores the programs in memory locations not occupied with the EP_{new} programs installed by said step of moving.

3. The method of claim 1, further comprising the steps of:

erasing said first area of said memory, said erasing step to be performed prior to said step of installing the EP_{new} programs into said first area of said memory; and

erasing said second area of said memory, said erasing step to be performed after said step of altering operation of the apparatus and prior to said step of installing the remaining programs of said P_{new} set of programs.

4. The method of claim 1, wherein said step of altering operation of said apparatus to execute said EP_{new} programs is accomplished by installing an offset address to pass control of said apparatus to said EP_{new} programs.

5. A method for installing a new set of communication programs P_{new} into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs P_{new} to said apparatus via said port, with the aid of a set of communications programs P_{old} already resident in said memory, where said set of programs P_{old} contains a subset of programs EP_{old} that occupy less than half of the memory and said set of programs P_{new} also contains a subset of programs EP_{new} that, when installed, occupy less than half of the memory, comprising the steps of:

installing the EP_{new} programs in a first area of said memory that contains programs other than the EP_{old} programs, thereby overwriting at least a portion of one program in said P_{old} set of programs;

altering operation of said apparatus to execute the EP_{new} programs instead of the EP_{old} programs;

moving the EP_{new} programs from said first area of memory to a second area of said memory; and

installing the remaining programs of said P_{new} set of programs in said first area of memory.

6. The method of claim 5, further comprising the step of:

erasing said first area of said memory, said erasing step to be performed prior to said step of installing the EP_{new} programs into said first area of said memory.

7. The method of claim 5, wherein said moving step further comprises the steps of:

copying the EP_{new} programs from said first area of memory to said second area of memory; and

erasing said first area of memory.

8. The method of claim 5, wherein said step of altering operation of said apparatus to execute said EP_{new} programs is accomplished by installing an offset address to pass control of said apparatus to said EP_{new} programs.

EXHIBIT B

Italics: Rembrandt's proposed terms
Underlined: Cable Parties' proposed terms

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
1. calling modem	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)[2]	Rembrandt does not believe this term requires construction. In the alternative: a communication device that begins the process of establishing or attempting to establish a connection with another communication device.	modem operable with ITU V. standards that places a call to an answering modem over a telephone network (*i.e.*, cellular or PSTN)
2. answering modem	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	Rembrandt does not believe this term requires construction. In the alternative: a communication device that responds to a connection attempt or request from a calling modem [defined above].	modem operable with ITU V. standards that answers a call placed over a telephone network (i.e. cellular or PSTN) by the calling modem

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[1] To distinguish the '627 patent All Other Parties, Cable Parties refers to the All Other Parties (Equipment Vendors and cable multiple systems operators ("MSOs")) adverse to Rembrandt on the Eight Patents in the parties' respective pleadings.

[2] For brevity, these charts identify the subpart for each independent claim that is the first instance where a term or phrase appears (or asserted dependent claim, if the phrase in question only appears in a dependent claim), rather than all instances where a term or phrase reappears within a claim. Each construction carries through the claim. In addition, this Joint Chart lists dependent claims at-issue that include the term or phrase, whether the term or phrase to be construed is part of the claim by dependence alone, or by dependence and express use in the dependent claim.

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
3. link layer	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	The second lowest layer of the Open Systems Interconnect (OSI) seven layer model, concerned with providing the functional and procedural means to transfer data between two communication devices, and to detect and correct errors that can occur in the physical layer.	second lowest layer of a communication protocol that performs error checking functions as well as retransmitting frames that are not received correctly *See rows 4 & 12 below* for the actual and complete claim language at issue.
4. establishing a link layer connection between a calling modem…and an answering modem	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	Rembrandt does not believe this term requires construction. In the alternative: applying link layer [defined above] parameters for the link layer Rembrandt does not believe this term requires construction. In the alternative: [defined above] for a connection between a calling modem [defined above] and an answering modem [defined above].	connection that is established after establishing the physical layer connection, without transferring data bytes by using telephone network link layer standards (*i.e.*, V.42, V.42bis or MNP)
5. physical layer	1(b), 3, 4, 5, 6(b), 8, 9, 10(b)	The lowest layer of the Open Systems Interconnect (OSI) seven layer model, concerned with establishing the mechanical, electrical, functional, and procedural connection between two communication devices.	The lowest layer of a communications protocol that is concerned with establishing the electrical and mechanical connection between two modems. *See rows 6-9 below* for the actual and complete claim language at-issue.
6. physical layer connection	1(b), 3, 4, 5, 6(b), 8,	Rembrandt does not believe this term requires construction. In the alternative: physical layer [defined above] parameters for a connection.	connection formed between the calling modem and answering modem upon completion of training and start-up, before any link layer connection is

U.S. Patent No. 5,852,631 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
		9, 10(b)		established
7.	physical layer modulation	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	A protocol that is concerned with establishing the mechanical, electrical, functional, and procedural connection between two communication devices.	a telephone network (*i.e.* PSTN or cellular) standard that governs only the establishment of physical layer connections between a calling and answering modem
8.	establishing a physical layer connection between said calling and said answering modems	1(b)	Rembrandt does not believe this term requires construction. In the alternative: applying physical layer [defined above] parameters for a connection between the calling modem [defined above] and the answering modem [defined above].	the modems use communication techniques different from data byte transfer (*e.g.* different frequency tones) to negotiate the physical layer modulation and to then establish the physical layer connection

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
9.	wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations	1(b), 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: wherein the physical layer connection [defined above] is based on the negotiated physical layer modulation chosen from the first and second physical layer modulations [defined above].	physical layer connection parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated
10.	means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation	6(b), 8, 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for establishing a physical layer connection between said calling and said answering modems" Function: Establishing a physical layer connection between the calling and answering modems. Structure: Control processor programmed to perform the steps of identifying and applying a commonly supported physical layer communication protocol between the calling and answering modems, or the equivalents. (FIG. 2 (40 and 42) and FIG. 9	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing a physical layer connection between said calling and said answering modems – *See row 5 above* physical layer connection -- *See row 7 above* physical layer modulation – *See row 8 above* wherein said physical layer connection is based on a negotiated physical layer modulation chosen from

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
chosen from said first and second physical layer modulations		(114, 124, 120, 124')	said first and second physical layer modulations – *See row 9 above* Structure – calling PSTN or cellular modem having a DSP that listens to and creates frequency tones in accordance with a control processor programmed to perform either the algorithm described in Figure 4 or 6, the control processor including a memory that stores the algorithm; answering PSTN or cellular modem having a DSP that listens to and creates frequency tones in accordance with a control processor programmed to perform either the algorithm described in Figure 5 or 7, the control processor including a memory that stores the algorithm
11. logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer	10(b)	Rembrandt does not believe this term requires construction. In the alternative: programming that allows a physical layer connection [defined above] between a calling modem [defined above] and an answering modem [defined above] to be applied based on the negotiated physical layer modulation chosen from the first and second physical layer modulations [defined above].	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations -- *See row 5 above for construction of this function*

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations			Structure – operating code for implementing either the algorithm of Figure 4 or Figure 6
12. establishing said link layer connection based upon said negotiated physical layer modulation	1(c), 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: applying link layer [defined above] parameters for a connection based on the negotiated physical layer modulation.	before the modems can transfer data bytes, the link layer parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated
13. means for establishing said link layer connection based upon said negotiated physical layer modulation	6(c), 8, 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for establishing said link layer connection based upon said negotiated physical layer modulation". Function: Establishing a link layer connection based	Means plus function element to be construed pursuant to 112, ¶ 6. Function – link layer parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated – *see row 12 above*

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
		upon a negotiated physical layer modulation. Structure: Control processor programmed to perform the step of establishing link layer parameters to default values that are based upon the previously negotiated physical layer modulation, or the equivalents. (FIG. 2 (44) and FIG. 9 (114, 124, 120, 124'))	Structure – control processor in the PSTN or cellular calling modem that operates an algorithm stored in its memory that sets link layer parameters to default values that were preset in the calling modem before the modems communicated if a particular physical layer modulation was negotiated; control processor in the answering PSTN or cellular modem that operates an algorithm stored in its memory that sets link layer parameters to default values that were preset in the answering modem before the modems communicated if a particular physical layer modulation was negotiated

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U.S. Patent No. 5,852,631 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES[1] CONSTRUCTION
14.	logic for establishing link layer connection based upon said negotiated physical layer modulation	10(c)	Rembrandt does not believe this term requires construction. In the alternative: programming that allows link layer [defined above] parameters for the connection to be applied based on the negotiated physical layer modulation.	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing link layer connection based on said negotiated physical layer modulation -- *see row 12 above* Structure – operating code for implementing an algorithm that causes a calling modem to default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated

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U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1. physical layer of a data connection	1(b), 2, 3, 6, 9(c), 10, 11, 14	Rembrandt does not believe this term requires construction. In the alternative: the parameters of the data connection associated with the physical layer [defined above].	ITU V. physical layer industry standard (e.g., V.22, V.22bis, V.32, V.32 bis, V.34) in existence as of May 31, 1995
2. to determine a set of parameters for the physical layer of the data connection with the far end data communications equipment	1(b), 2, 3, 6, 9(c), 10, 11, 14	Rembrandt does not believe this term requires construction. In the alternative: to identify a set of parameters to be used for the physical layer [defined above] of the data connection between two data communication devices.	before error control, the negotiated physical layer standard is used to determine the physical layer parameters of the data connection
3. error control negotiation sequence[s]	1(c), 2, 3, 6, 9(b), 10, 11, 14	A sequence of approaches that a communication device may employ concerning transmission errors, wherein the sequence of approaches may include at least one approach that takes no error control action. error control negotiation sequences: more than one error control negotiation sequence [defined above].	a sequence of different types of error control protocols or a disconnection step that the equipment attempts to use in turn, such that when an attempt to use one such protocol fails, the next option in the sequence is tried

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U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
_4._ error control	1(c), 2, 3, 6, 9(b), 10, 11, 14	Any of a variety of approaches employed concerning transmission errors that occur on a communications channel.	link layer error control protocol standards (LAPM, MNP, or Buffer) in existence as of May 31, 1995
_5._ selecting one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer	1(c), 2, 3, 6	Rembrandt does not believe this term requires construction. In the alternative: selecting an error control negotiation sequence [defined above] based upon the value of at least one parameter associated with the physical layer [defined above].	after negotiating the physical layer and determining the physical layer parameters, using the value of at least one determined physical layer parameter to select one of multiple link layer error control negotiation sequences
_6._ selects from memory one of a number of error control negotiation sequences as a function of a value of at least one parameter	9(d), 10, 11, 14	_see row 5 above_	_see row 5 above_

U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
from the set of parameters for the physical layer			
7. negotiating error control… in accordance with the selected one of the number of error control negotiation sequences	2	Rembrandt does not believe this term requires construction. In the alternative: selecting one of the approaches to error control from among those approaches available in the selected error control negotiation sequence [defined above].	executing the selected error control negotiation sequence to attempt to negotiate link layer error control parameters after the negotiation of the physical layer
8. negotiates error control… in accordance with the selected one of the number of error control negotiation sequences	10	*see row 7 above*	*see row 7 above*

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U.S. Patent No. 4,937,819 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1.	master unit	1(b), 2, 11, 12, 14(a)	Rembrandt does not believe this term requires construction. In the alternative: a data communication device that communicates with one or more modems.	device installed in a network that sends messages to its remote units using time division multiplexing without packet headers or delimiters
2.	remote units communicating with said master unit in a multidrop configuration	1(c), 2, 11, 12, 14	Rembrandt does not believe this term requires construction. In the alternative: modems that communicate with a master unit [defined above] in a network linking multiple units together.	configuration where all inbound transmissions to the master unit contain responses to outbound polls to modems that receive time division multiplexed messages without packet headers or delimiters from their master unit
3.	communication with a master unit in a multidrop configuration	14(a)	*see row 2 above*	*see row 2 above*

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U.S. Patent No. 4,937,819 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
_4._ application program[s]	1(d), 2, 11, 12, 14(a)	A computer program or process that can be run on a remote communication device, such as a modem.	program that directly meets the needs of a user, such as payroll, inventory control, word processing, accounting, spreadsheet, etc.
5. in a time slot assigned to each of said application programs	1(d), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: in one of the time slots assigned to the application programs [defined above].	each application program is assigned to a single time slot per subframe
6. said time slots	1(e)	said intervals of time	_see row 5 above_
_7._ time slot assigned to each of said application programs	1	An interval of time during which data from an application program may be transmitted.	_see row 5 above_
8. messages outbound from said master unit	1(d), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: the remote units get messages from the master unit [defined above].	messages sent from the master unit to remote units using time division multiplexing without packet headers or delimiters

U.S. Patent No. 4,937,819 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
9.	master network timing means	1(e), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: a process or device, such as a network timing control processor, that provides timing for the master unit [defined above].	network timing and control processor that stores user-input initialization parameters including network clock framing periods, slot and subframe assignments This is a "coined term" defined by the patent. Alternatively, if construed under Section 112, ¶6, it has this construction as its corresponding structure.
10.	a period which is divided into a plurality of subframes, wherein each subframe is divided into said time slots, and each of said time slots is used as an interval in which one of said application programs in	1(e), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: with a time period used by the master unit, the time period being logically divided into subframes [defined below], each of which being further divided into time slots, and where each time slot is assigned to an application program [defined above] associated with a remote unit as a time period within which that application program [defined above] may transmit.	during initialization, a fixed, repeating length of time called a frame is divided by a user into subframes, each of which is divided into the same number of time slots, where each time slot in a subframe is assigned by a user to a different application, whereby the subframes and time slot assignments repeat from frame to frame

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U.S. Patent No. 4,937,819 **Claim Limitation**	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
said one of said remote units is assigned to transmit			
11. dividing a period of a clock in said master unit into a number of subframes dividing each subframe into a number of slots, each corresponding to transmission times for one of said remote units and assigning a slot to each of said application programs in said one of said	14(c)	Rembrandt does not believe this term requires construction. In the alternative: a time period used by the master unit being logically divided into subframes [defined above], each of which being further divided into time slots, and where each time slot is assigned to an application program [defined above] associated with a remote unit as a time period within which that application program [defined above] may transmit.	*see row 10 above*

U.S. Patent No. 4,937,819 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
	remote units			
12.	subframe[s]	1(e), 2, 11, 12, 14(c)	Rembrandt does not believe this term requires construction. In the alternative: a portion of a time period.	division of a frame that contains a fixed number of time slots that must begin and end within the frame, assigned by a user to a single remote unit
13.	each corresponding to transmission times for one of said remote units	14(c)	Rembrandt does not believe this term requires construction. In the alternative: each time slot is a transmission time for one of the remote units.	"each" refers to each subframe -- *see row 12 above*
14.	ranging means	1(f), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: a device or process that communicates with the master network timing means [defined above] that determines the transmission times between the master unit [defined above] and each of the remote units and sends each of the respective remote units [defined above] the corresponding transmission time between the master unit and that remote unit.	Means plus function element to be construed pursuant to 112, ¶ 6. Function – communicating with said master network timing means wherein a transmission time between said master unit and each of said respective remote units is calculated and transmitted from said master unit to each of said respective remote units, each of said respective remote units using said transmission time to adjust initiation of said time slots

U.S. Patent No. 4,937,819 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
			Structure – network timing and control processor **12** (including library table), the ranging and network initialization generator **20**, and ranging receiver **32**, executing an algorithm to perform, during initialization of the master unit before the remote units transmit data, a ranging calculation for each combination of remote unit and application
15. reservation request generator	2	A device or process that adds to a message a request for additional time slots.	*See row 17 below* for construction of the complete and actual claim term at-issue: "reservation request generator which activates a reservation request bit for requesting an additional time interval inbound to said master unit"
<u>16.</u> reservation request bit	2, 11	Rembrandt does not believe this term requires construction. In the alternative: at least one bit in a message in order to indicate to the master unit [defined above] that the remote unit [defined above] wants additional time to be allocated to it for a message.	bit contained in each time slot in which a remote unit may transmit that allows the remote unit to request temporary use of preassigned time slots of subsequent remote units
<u>17.</u> reservation request generator which	2, 11	Rembrandt does not believe this term requires construction. In the alternative: a reservation request generator [defined above] in a remote unit that sets at	component in the remote unit that monitors a compression buffer for fields exceeding a preset parameter limit stored in the initialization parameter

U.S. Patent No. 4,937,819 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
activates a reservation request bit for requesting an additional time interval inbound to said master unit		least one bit in a message in order to indicate to the master unit [defined above] that the remote unit [defined above] wants additional time to be allocated to it for a message.	table, senses whether an application sending a message requires more than its one subframe time slot, and activates the reservation request bit in its time slot to request use of time slots assigned to subsequent remote units for the remainder of the message
18. reservation request processor	2	A device or process for receiving and processing requests for additional time slots from a reservation request generator.	*See row 18 below* for construction of the complete and actual claim term at-issue:: "reservation request processor communicating to said master network timing means, said reservation request processor being responsive to said reservation request bit"
19. reservation request processor communicating to said master network timing	2, 11	Rembrandt does not believe this term requires construction. In the alternative: a reservation request processor [defined above] communicating with the master network timing means [defined above] to process requests from remote units for additional time slots communicated from the remote units to the	a processor communicating to said master network timing means to allow a remote unit to request temporary use of preassigned time slots of subsequent remote units for transmitting messages that are longer than a single slot

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U.S. Patent No. 4,937,819 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
means, said reservation request processor being responsive to said reservation request bit		reservation request processor using reservation request bits.	
20. priority bit	11	A bit used to convey the relative importance of the communication.	a bit defining a remote unit's relative importance as compared to subsequent units, set by the user at initialization of the master unit
21. said time slot comprises a format so as to include a preamble, a poll response data bit, said reservation bits, at least one priority bit and error detection bit	11	Rembrandt does not believe this term requires construction. In the alternative: the time slot is formatted to include a preamble, a poll response data bit, reservation bits, at least one priority bit [defined above] and error detection bit.	the single time slot to which each application is assigned is formatted to include a preamble, a poll response data bit, said reservation request bits, at least one priority bit and error detection bit

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U.S. Patent No. 4,937,819 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
22. transmitting from said master unit to each of said respective remote units the transmission time between said master unit and said respective remote unit, each of said respective remote units using said transmission time to adjust initiation of said slots	14(d)	Rembrandt does not believe this term requires construction. In the alternative: the master unit [defined above] sends each remote unit [defined above], the transmission time between the master unit [defined above] and each respective remote unit, and each remote unit uses its transmission time (from the master unit [defined above] to that remote unit) to adjust when that remote unit initiates transmission.	during initialization of the master unit before the remote units transmit data, the master unit transmits to each remote unit the transmission time between the master unit and remote unit for each combination of remote unit and application

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1. data communications apparatus/communications apparatus/data communications equipment	1(a), 7(a), 8, 9(a), 10, 11(a), 15(a), 20(a), 26	Rembrandt does not believe this term requires construction. In the alternative: a data communication device.	network access unit (a single device that manages the flow of data between a local network and a network facility)
2. bus	1(b), 7(b), 8, 9(b), 10, 11(b), 15(a), 20(a), 26	Rembrandt does not believe this term requires construction. In the alternative: one or more conductors that are used as a path for transmitting information from any of several sources to any of several destinations.	hardware line(s) within a device used for data transfer among its components
3. time-division multiplexed bus	1(b), 7(b), 8, 9(b), 10, 11(b), 15(a), 20(a), 26	A bus having a bandwidth partitioned into a defined, repeated sequence of time slots, that is shared by two or more sources of data by limiting each source's transmission opportunities to discrete intervals of time.	a bus having its bandwidth partitioned into a repeating sequence of time slots defined to be used in the same way during each repetition, whereby only one data source can successfully transmit over the bus at any one discrete interval of time

U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
4. packet data	1(b), 7(d), 8, 9(d), 10, 11(d), 15(a), 20(a), 26	Variable bit rate data.	data that travels in packets
5. portion	1(b), 7(c), 8, 9(c), 10, 11(c), 15(c), 20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: a part of a whole.	fixed amount less than the whole
6. portion of the bandwidth is allotted to packet data	1(b)	Rembrandt does not believe this term requires construction. In the alternative: one or more time slots allotted to sources of packet data.	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel

U.S. Patent No. 5,719,858 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
7.	second portion of the predefined bandwidth	7(d), 9(d), 11(d)	Rembrandt does not believe this term requires construction. In the alternative: for transmitting packet data in a second portion of the predefined bandwidth [defined above].	*See row 6 above*
8.	the allocated portion of the bandwidth	15(d)	Rembrandt does not believe this term requires construction. In the alternative: the allocated time slot[s] of the bandwidth.	*See row 6 above*
9.	allocating a portion of the bandwidth of the time-division multiplexed bus to the plurality of packet data sources	15(c)	Rembrandt does not believe this term requires construction. In the alternative: allocating one or more time slots of the bandwidth of the time-division multiplexed bus [defined above] to the plurality of packet data [defined above] sources.	*See row 6 above*
10.	allocating a portion of the bandwidth of the time-division multiplexed bus	20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: allocating one or more time slots of the bandwidth of the time-division multiplexed bus [defined above].	*See row 6 above*

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
11. portion of the bandwidth	1, 15, 20	One or more time slots of the bandwidth.	*See rows 5 & 6 above*
12. portion of the predefined bandwidth	7, 9, 11	One or more time slots of the predefined bandwidth.	*See rows 5 & 6 above*
13. having a predefined bandwidth	7(b), 8, 9(b), 10, 11(b)	Rembrandt does not believe this term requires construction. In the alternative: having a predefined bandwidth [defined above].	first and second portions of the TDM bandwidth fixed during initialization
14. predefined bandwidth	7, 9, 11	A predefined amount of data that can be carried in a unit of time.	*See row 13 above*
15. [for communicating synchronous data in a] first portion of the predefined bandwidth	7(c), 8, 9(c), 10, 11(c)	Rembrandt does not believe this term requires construction. In the alternative: for transmitting synchronous data in a first part of the predefined bandwidth [defined above].	portion of the TDM data transfer capacity, fixed at initialization, in which all synchronous data from the plurality of synchronous data sources must travel, and in which only such synchronous data may travel

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U.S. Patent No. 5,719,858 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
16.	synchronous data	7, 8, 9, 11	Constant bit rate data.	data sent synchronously through TDM without packetization
17.	plurality of packet data sources coupled to the time division multiplexed bus	1(c), 7(d), 8, 9(d), 10, 11(d)	Rembrandt does not believe this term requires construction. In the alternative: more than one source of packet data that are operatively connected to the time-division-multiplexed bus.	circuit boards inside the apparatus that each has its own interface connected to the TDM bus that sends only packet data
18.	coupling a plurality of packet data sources to the time division multiplexed bus	15(b), 20(c), 26	Rembrandt does not believe this term requires construction. In the alternative: operatively connecting each of a number of sources of packet data to the time-division multiplexed bus [defined above].	*See row 17 above*
19.	A plurality of synchronous data sources coupled to the time-division multiplexed bus	7(c), 8, 9(c), 10, 11(c)	Rembrandt does not believe this term requires construction. In the alternative: more than one source of synchronous data that are operatively connected to the time-division-multiplexed bus [defined above].	circuit boards inside the apparatus that each has its own interface connected to the TDM bus that sends only synchronous data

U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
20. plurality of packet data sources…that share the allotted bandwidth for transmitting packet data	1(c)	Rembrandt does not believe this term requires construction. In the alternative: more than one source of packet data that each use time slots that are allotted to packet data.	without the need for a central packet manager, each packet data source treats the allotted bandwidth as a single channel by contending for use of the entire channel in which no time slot is assigned to any particular packet data source
21. where the plurality of packet data sources share the second portion of the predefined bandwidth for transmitting packet data	7(e), 8, 9(d), 10, 11(d)	Rembrandt does not believe this term requires construction. In the alternative: where more than one source of packet data may use the second portion of predefined bandwidth [defined above] to transmit packet data [defined above].	without the need for a central packet manager, each packet data source treats the second portion of the predefined bandwidth as a single channel by contending for use of the entire channel in which no time slot is assigned to any particular packet data source

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
22. in such a way that the allocated portion is shared among the plurality of packet data sources	15(c)	Rembrandt does not believe this term requires construction. In the alternative: in a manner so that only one source of packet data [defined above] should use any particular allotted time slot at any time.	without the need for a central packet manager, each packet data source treats the allocated portion as a single channel by contending for the entire channel in which no time slot is assigned to any particular packet data source
23. allocating a portion of the bandwidth of the time-division multiplexed bus as a multiple-access packet channel	20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: allocating a portion of the bandwidth [defined above] to be accessed and shared by multiple sources of packet data.	*See row 22 above*
24. distributed packet manager	1(d), 7(f), 8, 10, 15(e), 20(d), 26	A device, process or algorithm located within each packet data source, that controls how the packet data source accesses the time-division multiplexed bus.	component within each packet data source that permits it to share the allotted bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
25. wherein each one of the plurality of packet data sources includes interface circuitry to the time division multiplexed bus for synchronizing packet data to the time division multiplexed bus	10, 11(d)	Rembrandt does not believe this term requires construction. In the alternative: each of the multiple sources of packet data [defined above] is operatively connected to the time division multiplexed bus [defined above] using interface circuitry in a manner that allows packet data to be communicated from that source of packet data within an appropriate allotted time slot for that source of packet data.	circuitry within each packet data source that permits them to share the second portion of the predefined bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time
26. controlling access by said packet data sources to the allocated portion of the bandwidth via a distributed packet manager within each of said packet data sources	15(e), 20(d), 26	Rembrandt does not believe this term requires construction. In the alternative: each source of packet data using a distributed packet manager [defined above] within that source of packet data to control that source's access to an allocated portion of the bandwidth [defined above].	using a component within each packet data source that permits them to share the allocated portion of the bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at a time

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
27. allocate access to the allotted bandwidth among said packet data sources	1	Control access by each of the packet data [defined above] sources to a portion of the bandwidth previously assigned to packet data [defined above].	This language is the function of the "distributed packet manager." *See row 24 above*
28. allocate access to the second portion of the predefined bandwidth among said packet data sources	7	Control access by each of the packet data [defined above] sources to a portion of the predefined bandwidth [defined above].	This language is the function of the "distributed packet manager." *See row 24 above*
29. controlling [the] access by said packet data sources to the allocated portion of the bandwidth	15, 20	Controlling access by each of the packet data [defined above] sources to a the allocated portion of the bandwidth [defined below].	This language is the function of the "distributed packet manager." *See row 24 above*

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
30. the second portion of the predefined bandwidth being shared in such a way that only one of the plurality of packet data sources accesses the second portion of the predefined bandwidth at a time	9(d)	Rembrandt does not believe this term requires construction. In the alternative: the second portion of the predefined bandwidth [defined above] is used by the sources of packet data so that only one source of packet data should use any particular allotted time slot at a time.	sharing where only one packet data source can attempt to access the predefined second portion at a time
31. transmitting packet data from one of the plurality of packet data sources having access to the multiple-access packet channel	20(e), 26	Rembrandt does not believe this term requires construction. In the alternative: transmitting packet data [defined above] from one of the multiple sources of packet data [defined above] sources having access to the shared packet channel.	transmitting packet data from the only one of the plurality of packet data sources that was allowed by the distributed packet manager to have access to the multiple-access packet channel

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
_32._ network access manager/module	8, 26	A device, process or algorithm for controlling the assignment of synchronous and packet data portions on a time division multiplexed bus [defined above], and for passing data between the bus and a network.	component of the network access unit that provides the interface between the TDM bus in the network access unit and at least one network facility
33. a counter for counting time-slots representing the second portion of the predefined bandwidth	11(d)	Rembrandt does not believe this term requires construction. In the alternative: a device that measures time slots in the second portion of the predefined bandwidth [defined above].	a counter that counts only the time slots in the second portion of the predefined bandwidth

U.S. Patent No. 6,950,444 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1.	the preamble operating to frame the message and to delimit the message from silence	1(b), 12(b), 23(b), 24, 34(b), 35	Rembrandt does not believe this term requires construction. In the alternative: an initial pattern of bits to frame the message and to delimit the message from silence.	the preamble includes a first symbol transmitted at a power level higher than all other preamble symbols to precisely identify the beginning of the message and communication link control information used to precisely identify the end of the message
2.	a plurality of bits representing communication link control information	1(b), 12(b), 23(b), 24 34(b), 35	Rembrandt does not believe this term requires construction. In the alternative: multiple bits used to convey communication link control information [defined above].	transmit rate bits, maximum receive rate bits, address bits (where there is more than one remote), and message format bits, decoded by the receiver to control communications over the link
3.	communication link control information	1(b), 12(b), 23(b), 24 34(b), 35	A programmable pattern of bits to convey information regarding the communication.	*See row 2 above*
4.	means for applying a	23(b),	Means plus function term: "means for applying a preamble to a communication message".	Means plus function element to be construed pursuant to 112, ¶ 6.

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U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
preamble to a communication message…the preamble including a plurality of bits representing communication link control information	24	Function: Applying a preamble to a communication message. Structure: A sequencer and multiplexer, or the equivalents. FIG. 8 (elements 224 and 236).	Function – applying a preamble to a communication message, the preamble operating to frame the message and delimit the message from silence, the preamble including a plurality of bits representing communication link control information -- *See rows 1 & 2 above* for construction of limitations of this function Structure – includes transmit sequencer **236**, message format **201**, the remote address **202**, the receiving rate **204** and the transmission rate **205**, along with the multiplexer **214**. **201-202** and **204, 206** are computer readable memory that separately store bits representing the communication link control information (*See row 3 above*) and separately supply those bits to the multiplexer **214** when commanded to do so by the multiplexer
5.	an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per	1(c)	Rembrandt does not believe this term requires construction. In the alternative: a mechanism adapted to convert preamble bits into multiple symbols, where the symbols are encoded using a lower bit to symbol rate than the maximum rate capable of being supported over a communication channel [defined above].	an encoder converts the preamble bits into symbols at a lower bit per symbol rate than the maximum receive rate specified in the preamble that was just received

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U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT	CABLE PARTIES
		CONSTRUCTION	CONSTRUCTION
symbol rate relative to the maximum rate capable of being supported over a communication channel			

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U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
6. encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel	12(c), 34(c), 35	Rembrandt does not believe this term requires construction. In the alternative: converting the preamble bits into multiple symbols, where the symbols are encoded using a bit-to-symbol rate that is less than the maximum rate capable of being transmitted over a communication channel [defined above].	*See row 5 above*
7. the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel	12(c), 34(c) 35	Rembrandt does not believe this term requires construction. In the alternative: converting the preamble bits into multiple symbols, where the symbols are encoded using a bit-to-symbol rate that is less than the maximum rate capable of being transmitted over a communication channel [defined above].	*See row 5 above*

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U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
8. maximum rate capable of being transmitted over a communication channel/ maximum rate capable of being supported over a communication channel	1, 12, 23, 24, 34, 35	The highest bit per symbol rate at which the data portion of the message is sent.	*See row 5 above*
<u>9.</u> means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication	23(c), 24	<u>Means plus function term</u>: "means for encoding the preamble bits into a plurality of symbol indices". <u>Function</u>: Encoding the preamble bits into a plurality of symbol indices. <u>Structure</u>: A Preamble Encoder, or the equivalents. FIG. 8 (element 219)	Means plus function element to be construed pursuant to 112, ¶ 6. <u>Function</u> – encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel -- *See row 6 above* for construction of limitations of this function <u>Structure</u> – **219**, the 2 bit per symbol preamble encoder

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U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT	CABLE PARTIES
		CONSTRUCTION	CONSTRUCTION
channel			

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1. first transmitting means in the transmitting modem, including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency dependent characteristics of an output of said first transmitting means	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 15, 16, 17, 18, 19, 20	Rembrandt does not believe this term requires construction. In the alternative:

first transmitting means in the transmitting modem – a transmitter in the transmitting modem. including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency dependent characteristics of an output of said first transmitting means – means plus function claim language to be construed pursuant to 112, ¶ 6

Means plus function term: "adjusting means".

Function: Adjusting the frequency dependent characteristics of the output signal based upon the pre-emphasis coefficients.

Structure: A pre-filter, or the equivalents. (Fig. 5 (element 16).) | Means plus function element to be construed pursuant to 112, ¶ 6.

Structure – conventional modem transmitter **14**, with nine-tap filter **70** comprising delay blocks **71-79**, multipliers **81-89**, and adder **90**

Function – adjusting frequency dependent characteristics of an output of said first transmitting means |

U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
2. adjusting frequency [dependent] characteristics	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 15, 16, 17, 18, 19, 20, 21(c)	Rembrandt does not believe this term requires construction. In the alternative: adjusting the frequency dependent characteristics.	adjusting the signal using preemphasis coefficients computed from the noise spectrum parameters, so that the signal to be input into the receiving modem has a constant signal to noise ratio across all frequencies whether the noise is injected before or after the high frequency roll-off of a communications line
3. receiving means for receiving said output from said first transmitting means	1(c), 2, 3, 4, 5, 6(c), 7, 8(c), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "receiving means" Function: Receiving output from the transmitting means. Structure: A receiver, or the equivalents. (Fig. 5 (element "RX", between elements 22 and 24))	Means plus function element to be construed pursuant to 112, ¶ 6. Function – receiving said output from said first transmitting means Structure – Fig. 4, element "RX"

U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
4. noise spectrum	1(d), 2, 3, 4, 5, 6(d), 7, 8(d), 15, 16, 17, 18, 19, 20, 21(e)	Rembrandt does not believe this term requires construction. In the alternative: noise signal values.	frequency domain plot of the noise signals across a range of frequencies
5. generating means for generating parameters responsive to a noise spectrum of said output	1(d), 2, 3, 4, 5, 8(d), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "generating means for generating parameters responsive to a noise spectrum of said output" Function: Generating parameters responsive to a noise spectrum of the output signal. Structure: A discrete Fourier transform circuit, or the equivalents. (FIG. 4 (68); Col. 3: 41-45; Col. 4: 55-56).	Means plus function element to be construed pursuant to 112, ¶ 6. Function – generating parameters by choosing points of a noise spectrum of said output Structure – noise spectrum generator circuit **50**, including complex DFT block **68** that calculates a frequency domain plot of the noise signal at 709, 1145, 1800, 2455 and 2891 Hertz chosen from a 22 point discrete Fourier transform

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U.S. Patent No. 5,008,903 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
6.	generating means, including a noise spectrum generator circuit, for generating parameters responsive to a noise spectrum of said output	6(d), 7	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "generating means for generating parameters responsive to a noise spectrum of said output" Function: Generating parameters responsive to a noise spectrum of the output signal. Structure: Noise spectrum generator circuitry, or the equivalents. (Fig. 4, (element 50); FIG. 5 (element 24).)	*See row 5 above*
7.	parameters responsive to a noise spectrum/ parameters responsive to said noise spectrum	1, 6, 8, 21	Values based upon the noise signal at given frequencies.	generated parameters chosen as points of a noise spectrum of said output

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
8. said parameters	1(e), 2, 3, 4, 5, 6(e), 7, 8(e), 15, 16, 17, 18, 19, 20, 21(g)	Rembrandt does not believe this term requires construction. In the alternative: values based upon the noise spectrum [defined above].	*See row 7 above*
9. generating parameters responsive to said noise spectrum of said output	21(f)	Rembrandt does not believe this term requires construction. In the alternative: generating values based upon the noise spectrum [defined above] of the signal received from the transmitting modem.	generating parameters by choosing points of a noise spectrum of said output

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
10. means for calculating said noise spectrum of said output	1(d), 2, 3, 4, 5, 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for calculating said noise spectrum of said output". Function: Calculating said noise spectrum of said output. Structure: Noise spectrum generator circuitry, or the equivalents. (Fig. 4, (element 50); FIG. 5 (element 24).)	Means plus function element to be construed pursuant to 112, ¶ 6. Function – calculating noise signals of said output in the time domain and converting them into a spectrum in the frequency domain Structure – noise spectrum generator circuit **50**, including equalizers **56** & **57**, phase corrector **60**, slicer **62**, comparator **64**, inverse phase corrector **66** and block **68** that performs a 22 point discrete Fourier transformation calculation
11. noise spectrum generator circuit	6(g), 7, 8(g)	Rembrandt does not believe this term requires construction. In the alternative: circuitry that generates a noise spectrum [defined above].	circuit which calculates noise signals in the time domain (successive values corresponding to successive frequencies) and converts them into a spectrum in the frequency domain and generates parameters by choosing points of the noise spectrum
12. calculating a noise spectrum of said output	21(e)	Rembrandt does not believe this term requires construction. In the alternative: calculating a noise spectrum [defined above] of the signal received from the transmitting modem.	calculating noise signals of said output in the time domain and converting them into a spectrum in the frequency domain

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
13. second transmitting means for transmitting said parameters to the transmitting modem	1(e), 2, 3, 4, 5, 6(e), 7, 8(e), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "second transmitting means". Function: Transmitting said parameters to the transmitting modem. Structure: A second transmitter, or the equivalents. (Fig. 5 (element 38).)	Means plus function element to be construed pursuant to 112, ¶ 6. Function – transmitting said parameters to the transmitting modem Structure – low rate secondary channel transmitter **38** that transmits on a sideband of the primary channel at a low transmission rate through line **42**

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
14. secondary channel	15, 16	A second communication path provided by a transmission medium via either physical or electrical separation from a first communication path.	sideband of the primary channel
15. computing means for computing the pre-emphasis coefficients from said parameters	1(f), 2, 3, 4, 5, 6(f), 7, 8(f), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "computing means". Function: Computing the pre-emphasis coefficients from the parameters. Structure: compute/computer block 48 and operating code which performs the steps of computing the pre-emphasis coefficients from the parameters, or the equivalents. (Fig. 4 (element 48); Col. 4: 66, Col. 5: 17.)	Means plus function element to be construed pursuant to 112, ¶ 6. Function – computing at the transmitting modem pre-emphasis coefficients from said parameters Structure – transmitting modem circuitry containing comparator **28** that subtracts the previous frequency domain plot of the noise signal (previous parameters) stored in shift register **26** from the current plot (current parameters), multiplier **30** that divides the output of the comparator, compute block **48** implementing the log to linear algorithm at Col. 4:66 and the algorithms set forth at Col. 5:1-17; and including AGC circuit
16. output from said transmitting step	21(c)	Rembrandt does not believe this term requires construction. In the alternative: output signal from the transmitting modem.	output of modem transmitter to be adjusted responsive to the pre-emphasis coefficients

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U.S. Patent No. 5,008,903 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
17. receiving said output from said first transmitting means	21(d)	Rembrandt does not believe this term requires construction. In the alternative: receiving the output signal sent from the transmitting modem.	remote modem receives "said output from said transmitting step" as construed above

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1. said memory being of a type which may be completely updated in its entirety but which is not volatile	1(b), 2, 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten.	the system enables all contents in the system's non-volatile memory to be erased and overwritten during an update
2. said memory being completely updatable in its entirety but non-volatile	6(b), 7, 8(b), 9	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten.	*See row 1 above*
3. said memory being non-volatile and capable of being completely updated in its entirety	10(c), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten.	*See row 1 above*

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
4. said memory being of a type, which is completely updatable in its entirety but non-volatile	18(b), 19, 20, 21	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten.	*See row 1 above*
5. memory . . . not volatile memory . . . non-volatile	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 10(c), 11, 12, 13, 14, 15, 16, 17, 18(b), 19, 20, 21	AGREED: memory that retains its contents when power to the memory is disconnected.	AGREED: memory that retains its contents when power to the memory is disconnected
6. said memory being the only program memory in said [the] system	1(b), 2, 3, 4, 5, 6(b), 7	Rembrandt does not believe this term requires construction. In the alternative: the only memory used by the system for non-volatile storage of initialization programs.	the system's completely updateable nonvolatile memory is the only memory from which the system executes programs

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
7. program memory	1, 6	Updateable and non-volatile memory where initialization programs are stored.	*See row 6 above*
8. a set of programs stored in said memory that are executed when the system needs to be initialized	1(b), 2, 3, 4, 5, 6(b), 7	Rembrandt does not believe this term requires construction. In the alternative: the set of programs used by the system to initialize it.	the set of programs used by the system to initialize it, including the boot up program for the apparatus and programs needed to maintain communications between the apparatus and a remote processor, that are stored in and executed from nonvolatile memory when the system is powered on or re-booted
9. said memory containing programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication through said communication port	10(c), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: a program that, when executed, provides communication with remote devices via the communication port.	*See row 8 above*

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
10. a program module in said memory that, when activated by said processor, effects communication with said port	8(c), 9	Rembrandt does not believe this term requires construction. In the alternative: a set of instructions that, when executed by the processor, provides communication with remote devices via the communication port.	the set of programs that upon execution by the processor from the system's non-volatile memory, enable the system to boot-up and communicate with a remote processor through the communications port
11. set of program means stored in said memory that are activated when said system needs to be updated with a new set of programs	18(c), 19, 20, 21	Rembrandt does not believe this term requires construction. In the alternative: set of programs stored in the memory that, when executed, support updating the system with a new set of programs.	set of programs used by the system to initialize it, including the boot up program for the apparatus, programs needed to maintain communications between the apparatus and a remote processor, and subroutines for updating the system's programs, that are stored in and executed from nonvolatile memory when the system is powered on or re-booted

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
12. alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing	1(c), 2, 3, 4, 5	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "alterable storage means for holding a displacement multi-bit memory address". Function: holding a displacement multi-bit memory address. Structure: register 40 (col. 2, line 59, col. 4, lines 37-48).	Means plus function element to be construed pursuant to 112, 6. Function – storing an updateable multiple bit address that is added to a memory address supplied by the processor that changes the first nonvolatile memory location accessed by the processor when the system is powered on or re-booted Structure – updateable offset address register **40** connected to processor **10** and modifier circuit **30**
13. alterable memory means for storing a multi bit memory address that controls the starting address accessed by the processor when initializing	6(c), 7	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "alterable memory means for storing a multi-bit memory address". Function: storing a multi-bit memory address. Structure: register 40 (col. 2, line 59, col. 4, lines 37-48).	*See row 12 above*
14. alterable storage means for holding an offset memory	18(d), 19, 20, 21	Means plus function claim language to be construed pursuant to 112, ¶ 6.	Means plus function element to be construed pursuant to 112, ¶ 6.

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT	CABLE PARTIES
		CONSTRUCTION	**CONSTRUCTION**
address that is used to point to a starting address accessed by said processor when initializing		Means plus function term: alterable storage means for holding an offset memory address. Function: holding an offset memory address. Structure: Register 40. (col. 2, line 59, col. 4, lines 37-48).	Function – storing an updateable multiple bit address that is added to a memory address supplied by the processor that changes the first memory location accessed by the processor when the system is powered on or rebooted Structure – updateable offset address register **40** connected to and separate from processor **10** and modifier circuit **30**

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
15. means for receiving a trigger signal at a telecommunications input port of the system to begin execution of said programs	7	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for receiving a trigger signal" Function: Receiving a trigger signal. Structure: Processor 10 programmed to perform the step of monitoring data supplied to the telecommunications port. (Figs. 1 and 2, Col. 3 lines 1-4, 52-56).	Means plus function element to be construed pursuant to 112, ¶ 6. Function – receiving from a port that communicates with a remote processor a signal to begin executing from the non-volatile memory the set of programs that needs to be executed when the system is powered on or rebooted Structure[3] – processor 10 with port coupled to external communications line 12, buses 13, 14, and 16, register 40, modifier circuit 30, nonvolatile memory 20 containing EP set of programs, and an algorithm implementing steps in Figure 2 or 3 out of nonvolatile memory 20

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[3]   By way of example and without limitation, Cable Parties note that regarding claims 7, 8(d), and 10(d), there is no structure clearly linked to the claimed function, rendering the claims invalid. Cable Parties have set forth the only potentially corresponding structure.

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U.S. Patent No. 6,131,159 **Claim Limitation**	Claims at Issue	**REMBRANDT** **CONSTRUCTION**	**CABLE PARTIES** **CONSTRUCTION**
16. REMOVED		REMOVED -- INTENTIONALLY BLANK	REMOVED -- INTENTIONALLY BLANK
<u>17.</u> operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port	8(d), 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. <u>Means plus function term</u>: "operationally alterable means for setting the starting address" <u>Function</u>: Setting the starting address of program that effects communication with communication port. <u>Structure</u>: register 40 (col. 2, line 59, col. 4, lines 37-48).	Means plus function element to be construed pursuant to 112, ¶ 6. <u>Function</u> – while the program module in said memory is operating, downloading and storing an offset address that is added to a memory address supplied by the processor that changes the first memory location accessed by the processor when the system is powered on or rebooted <u>Structure</u> – processor **10** with port coupled to external communications line **12**, buses **13**, **14**, and **16**, offset address register **40**, modifier circuit **30**, nonvolatile memory **20** containing EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory **20**

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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
18. means for activating said program for controlling communication	10(d), 11, 12, 13, 14, 15, 16, 17	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for activating said program for controlling communication". Function: Activating program for controlling communication through communication port. Structure: Communication port and processor 10 programmed to perform the step of activating the program for controlling communication. (Figs. 1 and 2, Col. 3 lines 1-4, 16-19, 52-56).	Means plus function element to be construed pursuant to 112, ¶ 6. Function – activating the program in the nonvolatile memory for controlling communication through said communication port Structure – processor 10 with port coupled to external communications line 12, buses 13, 14, and 16, offset register 40, modifier circuit 30, nonvolatile memory 20 containing an EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory 20
19. means for... receiving information through said communication port to modify the programs in said memory, said information including the program for controlling	10(d), 11, 12, 13, 14, 15, 16, 17	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for…receiving information through said communication port". Function: Receiving information through the communication port. Structure: System including memory, communication port, and processor including programmed to perform the step of receiving	Means plus function element to be construed pursuant to 112, ¶ 6. Function – receiving in nonvolatile memory through the processor's communication port information which modifies the programs in the system's non-volatile memory, including the activated program for controlling communication in the nonvolatile memory, and a command received directly into the processor and executed Structure – processor 10 with port coupled to

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
communication through said communication port and a command that is executed by said processor effectively when it is received		information through said communication port to modify the programs in said memory. (Figs. 1 and 2, Col. 3 lines 1-4, 16-19, 52-56).	external communications line **12**, buses **13**, **14**, and **16**, offset register **40**, modifier circuit **30**, nonvolatile memory **20** containing an EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory **20**
20. communication[s] port coupled to said processor, said communication port being adapted to communicate with devices which are external to said system	8(b), 9, 10(b), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: an interface through which remote communication is supported, is operatively coupled to a processor to communicate with remote devices.	communications port connected to the processor so that the processor can receive program data, commands, and other information from remote devices through the port before any such information is stored in any memory
21. communication[s] port	8, 10, 11, 12, 13, 15, 16, 17	An interface through which remote communication is supported.	port through which information is downloaded from a remote processor into nonvolatile memory.

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U.S. Patent No. 5,778,234 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
1. a memory	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: electronic storage or holding place for data, including instructions.	nonvolatile memory
2. communications programs	1, 5	Programs that support remote communication.	*See rows 4-5 below* The term communications programs is used in the context of P_{old} and P_{new}
3. communication port	1, 5	An interface through which remote communication is supported.	port through which P_{new} programs are downloaded from a remote processor into nonvolatile memory
4. P_{old}	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: set of communication programs already resident in memory.	the entire set of programs used by the apparatus, which is stored in and executing from non-volatile memory, when the process to install a new entire set of programs begins
5. P_{new}	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a new set of programs to be installed.	the new entire set of programs (to replace P_{old}), which is stored in and executed from non-volatile memory after downloading into that memory through the communication port from a remote processor

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U.S. Patent No. 5,778,234 Claim Limitation		Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
6.	EP_{old}	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a subset of essential programs within P_{old} [defined above] that contains boot-up segments and program segments necessary to maintain communication between the apparatus and a remote device.	essential subset of the P_{old} set of programs that includes the boot up program for the apparatus and programs needed to maintain communications between the apparatus and a remote processor
7.	EP_{new}	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a subset of essential programs within P_{new} [defined above] that contains boot-up segments and program segments necessary to maintain communication between the apparatus and a remote device.	essential subset of the P_{new} set of programs that includes the new boot up program and new programs needed to maintain communications between the apparatus and a remote processor
8.	with the aid of a set of communication programs P_{old} already resident in said memory	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: some of the P_{old} programs [defined above] assist with installing P_{new} programs [defined above].	the P_{old} programs executing from the nonvolatile memory assist with downloading P_{new} programs for use in the nonvolatile memory
9.	installing the EP_{new} programs in a first area of said memory	1(b), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: downloading and storing the EP_{new} programs [defined above] into an area of memory [defined above] that does not contain the EP_{old} programs [defined above].	downloading and storing EP_{new} programs for immediate execution from a first area of said memory

U.S. Patent No. 5,778,234 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
10. said memory	1(b)(d), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a memory of the apparatus.	memory in which P_{old} is stored and executing
11. that contains programs other than the EP_{old} programs, thereby overwriting at least a portion of one program in said P_{old} set of programs	1(b), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: EP_{new} [defined above] is installed in an area of memory [defined above] that does not contain EP_{old} programs [defined above] and that includes at least a portion of at least one program in the P_{old} set of programs [defined above].	installing the EP_{new} programs in a first area of said memory that contains programs other than the EP_{old} programs overwrites at least a portion of one program in said P_{old} set of programs
12. altering operation of said apparatus to execute the EP_{new} programs instead of the EP_{old} programs	1(c), 2, 3, 4, 5(c), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: causing the apparatus to execute EP_{new} programs [defined above] instead of EP_{old} programs [defined above].	the apparatus stops executing the EP_{old} programs and immediately begins executing the EP_{new} programs from nonvolatile memory so that communications can continue seamlessly

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U.S. Patent No. 5,778,234 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION	CABLE PARTIES CONSTRUCTION
13. installing the remaining programs of said P_{new} set of programs	1(d), 2, 3, 4, 5(e), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: installing the remaining uninstalled programs of the P_{new} set of programs [defined above].	the EP_{new} programs are used to install the remaining programs of the P_{new} set of programs
14. remaining programs of said P_{new} set of programs	1(d), 2, 3, 4, 5(e), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: subset of P_{new} programs [defined above] that does not include the EP_{new} programs [defined above].	subset of P_{new} programs remaining to be transmitted that does not include the previously installed EP_{new} programs
15. altering operation of said apparatus to execute said EP_{new} programs is accomplished by installing an offset address to pass control of said apparatus to said EP_{new} programs	4, 8	Rembrandt does not believe this term requires construction. In the alternative: installing an offset address to cause the apparatus to execute the EP_{new} programs [defined above] instead of the EP_{old} programs [defined above].	installing an offset address that is added to a memory address supplied by the processor to cause the apparatus to stop executing the EP_{old} programs and immediately begin executing the EP_{new} programs from nonvolatile memory so that communications can continue seamlessly

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16. moving the EP_{new} programs from said first area of memory to a second area of said memory	5(d), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: moving the EP_{new} programs [defined above] into a second area of the memory [defined above].	the executing EP_{new} programs move into a second area of the nonvolatile memory

EXHIBIT C

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U.S. Patent No. 5,852,631

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Italics: Rembrandt's proposed terms
Underlined: Cable Parties' proposed terms

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		CONSTRUCTION AND INTRINSIC EVIDENCE	CONSTRUCTION AND INTRINSIC EVIDENCE
1. calling modem	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)[2]	Rembrandt does not believe this term requires construction. In the alternative: a communication device that begins the process of establishing or attempting to establish a connection with another communication device. Intrinsic Support: FIGS. 1, 2-8;	modem operable with ITU V. standards that places a call to an answering modem over a telephone network (*i.e.*, cellular or PSTN) Intrinsic Support: *See e.g.*, 1:55-61, 2:13-54, 2:61-63, 4:21-24; 5:9-16; 5:35-41; 5:42-63; 5:65-6:6; 6:12-24; 6:28-31; 6:32-36; 6:37-56; 7:2-13; 7:15-30; 7:35-37; 7:65-8:11;

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[1]   To distinguish the '627 patent All Other Parties, Cable Parties refers to the All Other Parties (Equipment Vendors and cable multiple systems operators ("MSOs")) adverse to Rembrandt on the Eight Patents in the parties' respective pleadings.

[2]   For brevity, these charts identify the subpart for each independent claim that is the first instance where a term or phrase appears (or asserted dependent claim, if the phrase in question only appears in a dependent claim), rather than all instances where a term or phrase reappears within a claim. Each construction carries through the claim. In addition, this Joint Chart lists dependent claims at-issue that include the term or phrase, whether the term or phrase to be construed is part of the claim by dependence alone, or by dependence and express use in the dependent claim.

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		After the cellular modem initiates the call, such that a communication link is established…" 6:26-30; "As depicted, the calling modem originates the call and establishes a communication link…" 9: 49-50; "Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model." 1:33-36; "The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer." 1:42-46; "Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 4:20-24; "As is well known, a variety of standards exist which govern the protocols for communication between modems." 1:55-56	8:12-23; 8:L26-30; 8: 41-47; 9:12-15; 9:28-37; 9:49-68; 10:1-7; 10: 24-31; 10:39-52; 11:30-58 ; 10:57-65; 11:11-21;l 11:52-58; 11:65-12:8; 12:29-35; 12:55-61; 13:15-22; 13:42-46 Figs. 1-9 V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42 and V.42 bis, are identifiers of differing communications standards." (1:55-62.) "cellular call" (2:27); "phone company" (5:37); "1-800 number" (5:39); "busy signal" (Fig.4); "calling signals" (7:15); "exchange of tones" over a phone connection (7:27). "Also, and as illustrated at block 67, the calling modem will abort the attempted communication if a busy signal is received." (9:12-15.)

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U.S. Patent No. 5,852,631 **Claim Limitation**	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		"It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention" 4:8-12; "The following description is of the best presently contemplated mode of carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention." 3:65-4:3; "As illustrated in FIG. 4 (assuming the calling modem is a cellular modem)…" 7:43-44; "After the cellular modem initiates the call, such that a communication link is established…" 6:26-30 "As depicted, the calling modem originates the call and establishes a communication link…" 9: 49-50. "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication	"The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor chip." (6:6-11.) "through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44." (7:23-30.) "As will be described in more detail in connection with the flowcharts of FIGS. 4-7, this signal may comprise a 1900 hertz tone, or alternatively may comprise a 1500 hertz tone modulated with a 1900 hertz tone. If only a 1900 hertz tone is transmitted as Ciqck signal 50, then the answer modem knows that the calling modem is configured as a Central Site, four-wire modem (see FIG. 6). Alternatively, if the Ciqck signal includes both 1500 and 1900 hertz components, then the answer modem knows that the calling modem is configured as a cellular modem." (7:5-13.) "The modems may also operate during this period to train their internal echo cancellers by, for example,

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two	ranging the established link of communication." (6:43-44.) "If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fallback error protocols provided by the calling modem, such as in the case of V.42, where MNP is a fall-back error-correcting protocol. Alternatively, if the answer modem does not support V.42 nor MNP, then **no** error-correcting protocol is established and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems." 11:59-12:8. See also '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. See also '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5)	

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and	

U.S. Patent No. 5,852,631 **Claim Limitation**	Claims at Issue	REMBRANDT **CONSTRUCTION AND INTRINSIC EVIDENCE**	CABLE PARTIES[1] **CONSTRUCTION AND INTRINSIC EVIDENCE**
		several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the	

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U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		CONSTRUCTION AND INTRINSIC EVIDENCE	CONSTRUCTION AND INTRINSIC EVIDENCE
		calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem;	

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is of the best presently contemplated mode of carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention. Consequently, the scope of the invention should be determined by referencing the appended claims. The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system	

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly. I. Physical Layer Connection Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 3:65-4:24; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of	

U.S. Patent No. 5,852,631 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES[1]** **CONSTRUCTION AND INTRINSIC EVIDENCE**
		the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and startup in accordance with the fast connect communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11;	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		"FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40." 6:26-30; "As depicted, the calling modem originates the call and establishes a communication link at block 80." 9:49-50; "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and establishing said link layer connection based upon	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention	

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		between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10	
2. answering modem	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	Rembrandt does not believe this term requires construction. In the alternative: a communication device that responds to a connection attempt or request from a calling modem [defined above]. Intrinsic Support: FIGS. 1, 2-8;	modem operable with ITU V. standards that answers a call placed over a telephone network (*i.e.* cellular or PSTN) by the calling modem Intrinsic Support: *See e.g.*, 1:55-61, 2:13-54, 2:61-63, 4:21-24; 5:9-16; 5:35-41; 5:42-63; 5:65-6:6; 6:12-24; 6:28-31; 6:32-36; 6:37-56; 7:2-13; 7:15-30; 7:35-37; 7:65-8:11;

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection. 2:62-15;	8:12-23; 8:L26-30; 8: 41-47; 9:12-15; 9:28-37; 9:49-68; 10:1-7; 10: 24-31; 10:39-52; 11:30-58 ; 10:57-65; 11:11-21;l 11:52-58; 11:65-12:8; 12:29-35; 12:55-61; 13:15-22; 13:42-46 Figs. 1-9 V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42 and V.42 bis, are identifiers of differing communications standards." (1:55-62.) "cellular call" (2:27); "phone company" (5:37); "1-800 number" (5:39); "busy signal" (Fig.4); "calling signals" (7:15); "exchange of tones" over a phone connection (7:27). "Also, and as illustrated at block 67, the calling modem will abort the attempted communication if a busy signal is received." (9:12-15.)

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		"In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer,	"The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor chip." (6:6-11.) "through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44." (7:23-30.) "As will be described in more detail in connection with the flowcharts of FIGS. 4-7, this signal may comprise a 1900 hertz tone, or alternatively may comprise a 1500 hertz tone modulated with a 1900 hertz tone. If only a 1900 hertz tone is transmitted as Ciqck signal 50, then the answer modem knows that the calling modem is configured as a Central Site, four-wire modem (see FIG. 6). Alternatively, if the Ciqck signal includes both 1500 and 1900 hertz components, then the answer modem knows that the calling modem is configured as a cellular modem." (7:5-13.) "The modems may also operate during this period to train their internal echo cancellers by, for example,

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		a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of	ranging the established link of communication." (6:43-44.) "If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fallback error protocols provided by the calling modem, such as in the case of V.42, where MNP is a fall-back error-correcting protocol. <u>Alternatively, if the answer modem does not support V.42 nor MNP, then **no** error-correcting protocol is established</u> and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems." 11:59-12:8. *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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		operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient	

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		operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first	

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		physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic	

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		mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58;

"The following description is of the best presently contemplated mode of carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention. | |

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		Consequently, the scope of the invention should be determined by referencing the appended claims. The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly. I. Physical Layer Connection Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 3:65-4:24; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable	

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		for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and	

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		startup in accordance with the fast connect communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol	

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		is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11; "FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40." 6:26-30; "As depicted, the calling modem originates the call and establishes a communication link at block 80." 9:49-50; "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of:	

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		establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer	

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| | | modulation.
7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and
logic for establishing link layer connection based upon said negotiated physical layer modulation."
claims 1, 2, 6, 7, 10 | |
| *3.* | link layer | 1(a), 3, 4, 5, 6(a), 8, | The second lowest layer of the Open Systems Interconnect (OSI) seven layer model, concerned with providing the functional and procedural means | second lowest layer of a communication protocol that performs error checking functions as well as retransmitting frames that are not received correctly |

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	9, 10(a)	to transfer data between two communication devices, and to detect and correct errors that can occur in the physical layer.	*See* rows 4 & 12 below for the actual and complete claim language at-issue. Intrinsic Support: "The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly." (1:51-54) *See also* 1:24-61 *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.
4. establishing a	1(a), 3,	Rembrandt does not believe this term requires	connection that is established after establishing the

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link layer connection between a calling modem…and an answering modem	4, 5, 6(a), 8, 9, 10(a)	construction. In the alternative: applying link layer [defined above] parameters for the link layer Rembrandt does not believe this term requires construction. In the alternative: [defined above] for a connection between a calling modem [defined above] and an answering modem [defined above]. Intrinsic Support: FIGS. 1, 2-8; "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and	physical layer connection, without transferring data bytes by using telephone network link layer standards (*i.e.*, V.42, V.42bis or MNP) Intrinsic Support: "*McGlynn* makes no suggestion of negotiating for features utilized prior to the data transfer mode of operation. Hence, *McGlynn* fails to disclose the step of establishing a link layer connection based on the negotiated physical layer modulation." (1/28/98 Response at 5.) "Not only does *McGlynn* fail to teach the principles of the present invention, but *McGlynn* specifically teaches away from the present invention. As noted hereinabove, *McGlynn* discloses a system to negotiate for features after a physical layer and a link layer have already been established, and *McGlynn* negotiates for features through the transfer of data bytes which are not transmitted prior to the establishment of physical and link layer connections." (1/28/98 Response at 6.) "[N]egotiation for features via the use of data byte transfer suggests that the physical layer and link layer should be already established before any

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		the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing	feature negotiation under *McGlynn* occurs in order to enable the transfer of data bytes. This is contrary to the present invention which uses different communication techniques (e.g., different frequency tones) to establish the physical and link layer connections <u>since data byte transfer is not yet enabled during the establishment of the physical and link layers</u>." (1/28/98 Response at 7.) *See also* Cited Prior Art. "Of particular relevance to the present invention is the ITU Standard V.42 (hereinafter referred to as V.42). The V.42 standard is intended for use in establishing the error-correcting protocol of the data link layer connection." (2:39-55.) "If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fallback error protocols provided by the calling modem, such as in the case of V.42, where MNP is a fall-back error-correcting protocol. Alternatively, <u>if the answer modem does not support V.42 nor MNP, then **no** error-correcting protocol is established</u> and a connect message is issued by the modems to their respective

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		communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to	digital terminal equipment so that user data can be transmitted between the two modems." 11:59-12:8. *See e.g.*, 1:55-61, 2:13-54, 2:61-63, 4:21-24; 5:9-16; 5:35-41; 5:42-63; 5:65-6:6; 6:12-24; 6:28-31; 6:32-36; 6:37-56; 7:2-13; 7:15-30; 7:35-37; 7:65-8:11; 8:12-23; 8:L26-30; 8: 41-47; 9:12-15; 9:28-37; 9:49-68; 10:1-7; 10: 24-31; 10:39-52; 11:30-58 ; 10:57-65; 11:11-21;l 11:52-58; 11:65-12:8; 12:29-35; 12:55-61; 13:15-22; 13:42-46 Figs. 1-9 V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of

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		the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick	Allowability.

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		Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated	

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		physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with	

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		a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established	

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		communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and startup in accordance with the fast connect communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of	

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		communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11; "FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40." 6:26-30; "As depicted, the calling modem originates the call and establishes a communication link at block 80." 9:49-50;	

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		"1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections,	

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		comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from	

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		said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10	
5. physical layer	1(b), 3, 4, 5, 6(b), 8, 9, 10(b)	The lowest layer of the Open Systems Interconnect (OSI) seven layer model, concerned with establishing the mechanical, electrical, functional, and procedural connection between two communication devices. Intrinsic Support: "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it.	The lowest layer of a communications protocol that is concerned with establishing the electrical and mechanical connection between two modems. *See* rows 6-9 below for the actual and complete claim language at-issue Intrinsic Support: "The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems." (1:49-51) *See also* 1:24-61 *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98

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		Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems.

The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. | Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment.

See also '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability. |

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		As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model." 1:23-61; "The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6)	

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		exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular	

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		call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second. Of particular relevance to the present invention is the ITU Standard V.42 (hereinafter referred to as V.42). The V.42 standard is intended for use in establishing the error-correcting protocol of the data link layer connection. The V.42 standard includes a detection phase which determines whether both modems are capable of a an error-corrected connection, an exchanging identification phase for determining error-correcting parameter values and a link establishment phase for establishing the error-corrected connection. Under normal circumstances, V.42 requires approximately 1-3 seconds to	

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		establish an error-corrected connection. While this is relatively small in comparison to the establishment of a physical layer connection under V.34, it can essentially double the connection time when used in conjunction with fast connect modems." 1:62-2:54; "Therefore, a heretofore unaddressed need exists in the industry for a system and method that reduces or eliminates the time required to establish a link layer connection so as to minimize the amount of time for establishing a connection between two modems." "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes	

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		establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." "The link layer is the second layer of the ISO model protocol stack and includes negotiating and establishing an error-correcting connection such as with ITU Standard V.42 or Microcom Networking Protocol (MNP). The link layer connection follows the physical layer connection and uses the physical layer in establishing the error-corrected connection. It is noted, however, that conventional wisdom to date has maintained the link layer connection be independent of the physical layer connection when establishing a connection between two modems. In contrast, the present invention establishes the link	

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		layer connection based upon the modulation chosen in the physical layer connection during the automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer connection is established substantially instantaneously upon the completion of the physical layer negotiation. This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure. By way of example, the ITU Standard V.42 (hereafter referred to as V.42) comprises a detection phase, and exchange identification (XID) phase, and a link establishment phase, all of which are briefly discussed below. A more detailed explanation of V.42 can be found in the publicly-available ITU (CCITT) Recommended Standard V.42 documentation." 11:30-58; "The detection phase is provided to determine whether the answer modem supports an error-correcting protocol. This phase is designed to avoid	

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		the potential disruptions to the answer DTE that could occur if the calling modem immediately enters the XID phase and the answering modem was not capable of an error-correcting communication. However, the detection phase is optional and may be disabled. If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fall-back error protocols provided by the calling modem, such as in the case of V.42, where MNP is provided as a fall-back error-correcting protocol. Alternatively, if the answer modem does not support V.42 nor MNP, then no error-correcting protocol is established and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems. The XID phase is provided for the negotiation of the error-correcting parameter values. These parameters essentially govern the error-correcting operation of the modems once the connection is established. As with the detection phase, the XID phase may be omitted if default parameter values are acceptable. For example, the following are provided as the default parameters values in the V.42 standard: Standard Reject, 16 bit FCS (Frame Check	

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		Sequence), V.42bis compression disabled, Frame Length (N401) of 128 octets, and Window Size (k) of 15 frames. However, the default settings are more often than not undesirable because, for example, most modems wish to negotiate Selective Reject, V.42bis data compression, and longer Frame Lengths and Window Sizes. Lastly, the link establishment phase is provided for actually making the error-corrected connection between the two modems. In V.42, this is implemented via a set asynchronous balanced mode extended (SABME) command. The SABME command is used to place the addressed error-corrected entity (i.e., the answering modem) into the connected state. The error-correcting entity then confirms acceptance of the SABME command by the transmission of an unnumbered acknowledgment (UA) response. By acceptance of this command, the error-corrected connection is essentially established and the modems then send a connect message to their respective data terminal equipment, such as computer 15 (FIG. 1). Unlike the detection phase and the XID phase, the link establishment phase is not optional and must be	

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		performed under V.42. Thus, in a best case scenario, only the link establishment phase is performed, which takes approximately 0.5 seconds. If all three phases are performed, then the link layer connection may take three or more seconds. Therefore, establishing an error-corrected connection with V.42 can take up to three seconds, depending on what defaults are set in the system. While this amount of time does not seem significant relative to the time required for establishing a physical layer connection via V.34 modulation (e.g., approximately 10-15 seconds), it is considerably more noticeable when a fast connect protocol is utilized that can establish a physical layer connection in about 1 second. Thus, when using a fast connect protocol, the error-correction negotiation can easily double the connect time, not to mention introduce a greater opportunity for failure by requiring additional handshaking. Accordingly, the present invention enables an error-corrected connection without having to perform the steps described above with regard to V.42, or those steps associated with other error-correcting protocols as known in the art. The present invention	

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		achieves this by presetting the XID phase parameters to default values that are based upon the negotiated physical layer connection. Therefore, when two multi-mode modems negotiate a physical layer connection, the link layer connection can be immediately established based upon the negotiated physical layer modulation. For example, in the embodiment described above in Section I, the exchange of tones in the mode synchronization sequence 40 indicates to each modem the type of modem it is communicating with, and therefore, certain assumptions can then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection. In the preferred embodiment of the present invention with the V.42 standard, the following parameters are set to the indicated default values when the two modems are capable of the fast connect sequence described above: Selective Reject, 16 bit FCS, 64 bit Maximum Frame Size (transmit and receive directions), 8 Frame Window Size (transmit and receive directions), V.42bis enabled, and 1,024 bit dictionary (transmit and receive directions). It should be noted, however, that one of ordinary skill in the art would recognize that these default values	

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		are merely illustrative settings and that different default values can be used. Moreover, each different type of connect sequence would preferably have its own set of default values. If it is determined by the modems in the mode synchronization sequence 40 that one or the other is not capable of a fast connect as described above, then the modems essentially fallback and perform an alternative error-correction sequence such as the recommended ITU Standard V.42 error-correction sequence. With reference to FIG. 8, a graphical illustration is provided of two fast connect modems in a first connect sequence 102 where error-correction negotiation is performed without the present invention and a second connect sequence 104 where the error-correction negotiation is performed with the present invention. As shown, following the mode synchronization sequence (also referred to as automode) 40 and the training and start-up sequence 42, the connect sequence 102 performs error-correction negotiation 44 which essentially doubles the time required for a connection to be established so as to allow user data 106 to be exchanged. In comparison, the connect sequence 104 in accordance with the present invention is able to	

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		establish a connection in essentially half the time by eliminating the error-correction negotiation 44. Thus, by establishing the error-correction parameters to default values in accordance with the type of physical error-connection determined by the automode sequence 40, a faster and more reliable connection is established." 11:59-13:41.	
6. physical layer connection	1(b), 3, 4, 5, 6(b), 8, 9, 10(b)	Rembrandt does not believe this term requires construction. In the alternative: physical layer [defined above] parameters for a connection. Intrinsic Support: FIGS. 1, 2-8; "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest	connection formed between the calling modem and answering modem upon completion of training and start-up, before any link layer connection is established. Intrinsic Support: "Once the modems have synchronized their communication protocol, or modulation standard, then they enter a training and startup sequence 42. . .. The completion of this sequence signifies the establishment of a physical layer connection between two modems. After the physical layer has been established, the communicating modems enter the information exchange/communication sequence,

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		layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest	referred to herein as error-correction negotiation 44, in order to establish the link layer connection." (6:37-64; *see generally* Fig. 2 and 6:26-64.) "At the completion of the training and start-up sequence 42, the modems have established a physical layer connection and are ready to establish the second layer connection, referred to as the link layer connection, via an error correction negotiation sequence 44 in accordance with the present invention. . .." (11:22-27.) "The link layer connection follows the physical layer connection and uses the physical layer in establishing the error-corrected connection. . . . [T]he present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection during the automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer connection is established substantially instantaneously upon completion of the physical layer negotiation." (11:33-46.) "Since the negotiations in *McGlynn* occur

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		layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6)	subsequent to the 'conventional or standard handshaking sequences' of the training and start up sequence, then the negotiations in *McGlynn* necessarily occur subsequent to the establishment of physical layer modulation which. . . occurs prior to the training and start up sequence." (10/28/97 Response at 10.) V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability. *See also* Cited Prior Art.

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		exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time	

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		of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the	

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		physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the	

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		operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast	

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		connect modem system described herein, for example, with modems that connect slowly. I. Physical Layer Connection Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 4:5-24; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and startup in accordance with the fast connect communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention	

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		will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11;	

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		"FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40." 6:26-30; "As depicted, the calling modem originates the call and establishes a communication link at block 80." 9:49-50; "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10	
7.	physical layer modulation	1(a), 3, 4, 5, 6(a), 8, 9, 10(a)	A protocol that is concerned with establishing the mechanical, electrical, functional, and procedural connection between two communication devices. Intrinsic Support: FIGS. 1, 2-8.	a telephone network (*i.e.*, PSTN or cellular) standard that governs only the establishment of physical layer connections between a calling and answering modem Intrinsic Support: FIGS. 1-9

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		"In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application	"Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model." (1:60-61.) "Once the modems have synchronized their communication protocol, or modulation standard, then they enter a training and startup sequence 42. . .. The completion of this sequence signifies the establishment of a physical layer connection between two modems. After the physical layer has been established, the communicating modems enter the information exchange/communication sequence, referred to herein as error-correction negotiation 44, in order to establish the link layer connection. This is of particular relevance to the present invention in that it includes negotiation of a error-correcting protocol such as V.42 . . . ." (6:37-65; *see generally* Fig. 2 and 6:26-64.) *See e.g.*, 1:55-61, 2:13-54, 2:61-63, 4:21-24; 5:9-16; 5:35-41; 5:42-63; 5:65-6:6; 6:12-24; 6:28-31; 6:32-36; 6:37-56; 7:2-13; 7:15-30; 7:35-37; 7:65-8:11; 8:12-23; 8:L26-30; 8: 41-47; 9:12-15; 9:28-37; 9:49-68; 10:1-7; 10: 24-31; 10:39-52; 11:30-58 ; 10:57-65; 11:11-21;l 11:52-58; 11:65-12:8; 12:29-35; 12:55-61; 13:15-22; 13:42-46

U.S. Patent No. 5,852,631 **Claim Limitation**	Claims at Issue	REMBRANDT **CONSTRUCTION AND INTRINSIC EVIDENCE**	CABLE PARTIES[1] **CONSTRUCTION AND INTRINSIC EVIDENCE**
		layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for	V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the	

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of	

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2;	

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is of the best presently contemplated mode of carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention. Consequently, the scope of the invention should be	

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		determined by referencing the appended claims. The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly. I. Physical Layer Connection Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 3:65-4:24; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and startup in accordance with the fast connect	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol	

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11; "Turning now to the drawings, FIG. 1 shows a system diagram of a system illustrating multiple modems intercommunicating through a variety of mediums, including cellular and PSTN." 4:20-24; "As is well known, a variety of standards exist which govern the protocols for communication between modems." 1:55-56; "It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention" 4:8-12; "The following description is of the best presently contemplated mode of carrying out the present invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of describing the general principles of the invention." 3:65-4:3;	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		"As illustrated in FIG. 4 (assuming the calling modem is a cellular modem)…" 7:43-44; "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections	

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		and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation. 10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising:	

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10 '631 Patent File History Office Action of September 4, 1997; Response of October 23, 1997.	
8. establishing a physical layer connection between said calling and said answering modems	1(b)	Rembrandt does not believe this term requires construction. In the alternative: applying physical layer [defined above] parameters for a connection between the calling modem [defined above] and the answering modem [defined above]. Intrinsic Support: FIGS. 1, 2-8; "In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection during the	the modems use communication techniques different from data byte transfer (*e.g.*, different frequency tones) to negotiate the physical layer modulation and to then establish the physical layer connection Intrinsic Support: FIGS. 4-7 "In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer connection is established substantially instantaneously upon the completion of the physical layer negotiation. This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure." 11: 36 – 51 "If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fall-back error protocols provided by the calling modem, such as in the case of V.42, where MNP is provided as a fall-back error-correcting protocol. Alternatively, if the answer modem does not support V.42 nor MNP, then no error-correcting protocol is established and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems." 11:64-12:8	of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." (6:6-11.) "Indeed, the significance of the fast connect protocol is achieved when both the calling modem and the answer modem are capable of communicating in accordance with the fast connect modulation protocol herein described so that through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44." (7:23-30.) "Accordingly, at the completion of the automatic mode synchronization sequence 40 (FIG. 2), the modems enter into a training and start-up sequence 42. As mentioned above, in the training and startup sequence 42 the modems test the established communication link for noise, bandwidth, etc., in order to determine the appropriate rate for communication. This is performed using the modulation scheme determined in the automatic mode synchronization sequence 40 as illustrated in FIGS. 4, 5, 6, and 7." (10:57-65.)

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		See above support for physical layer modulation. "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five layer model comprises the following layers from	"For example, in the embodiment described above in Section I, the exchange of tones in the mode synchronization sequence 40 indicates to each modem the type of modem it is communicating with, and therefore, certain assumptions can then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:65-13:4.) "*McGlynn* negotiates for features by simply transmitting data bytes between the two modems. . .. Accordingly, *McGlynn* uses previously established physical layer and link layer connections to perform feature negotiation." (1/28/98 Response at 4.) "*McGlynn* specifically teaches away from the present invention. … *McGlynn* negotiates for features through the transfer of data bytes which are not transmitted prior to the establishment of physical and link layer connections. … This is contrary to the present invention which uses different communication techniques (e.g., different frequency tones) to establish the physical and link layer connections since data byte transfer is not yet enabled during the establishment of the physical and

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34 standard includes the following primary	link layers." (1/28/98 Response at 6-7.) *See also* Cited Prior Art. "Particularly, the probing and ranging sequences are bypassed and the file parameters are assumed in ITU Standard V.8, INFO0, and INFO1. As an example, in ITU Standard V.8, the data call, the LAPM and the full-duplex training parameters are preset to default values if the tones exchanged during automode sequence indicate that both modems are capable of fast connect operation. . . ." (11:11-21.) *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating modems, it nevertheless possesses several	

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for establishing a link layer connection between a	

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U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem; FIG. 3 is a timing diagram similar to FIG. 2,	

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		illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable for operating in conjunction with the present	

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		invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18; "By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and startup in accordance with the fast connect	

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		communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is	

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		accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip." 5:42-6:11; "FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40. During this period, the modems exchange parameters that identify the modems, and thus, their communication protocol. This sequence 40, thus, synchronizes the modems for communication in accordance with the same standard or protocol, such as V.34, V.22, V.22bis, etc." 6:26-36; "As will be appreciated by those of ordinary skill in the art, other calling signals may be transmitted by the calling modem. For example, calling signals consistent with that of a facsimile transmission, or calling signals consistent with other modem modulation standards, such as V.34, V.32, V.32bis, etc., may be transmitted. Since automatic	

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		connection and synchronization to facsimile, and these other modulation standards, are well known it will not be discussed herein." 7:14-22; "As depicted, the calling modem originates the call and establishes a communication link at block 80." 9:49-50; "It is noted, however, that conventional wisdom to date has maintained the link layer connection be independent of the physical layer connection when establishing a connection between two modems. In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection during the automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer connection is established substantially instantaneously upon the completion of the physical layer negotiation. This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure."	

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		11:36-51; "However, the detection phase is optional and may be disabled. If the call modem determines that the answering modem does not support a V.42 error-correcting protocol, there are often times fall-back error protocols provided by the calling modem, such as in the case of V.42, where MNP is provided as a fall-back error-correcting protocol. Alternatively, if the answer modem does not support V.42 nor MNP, then no error-correcting protocol is established and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems." 11:64-12:8; "However, each modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. In the context of the present disclosure, a memory device is a computer readable medium that is embodied in an electronic, magnetic, optical or other physical device or means that can contain or store a computer program, such as the	

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		operating code for the modem 20, 24, for use by or in connection with a computer related system or method. The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." 13:58-14:10 "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations;	

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		and establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer	

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		program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10	

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9. wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations	1(b), 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: wherein the physical layer connection [defined above] is based on the negotiated physical layer modulation chosen from the first and second physical layer modulations [defined above]. Intrinsic Support: See above support for physical layer modulation. During this period, the modems exchange parameters that identify the modems, and thus, their communication protocol. This sequence 40, thus, synchronizes the modems for communication in accordance with the same standard or protocol, such as V.34, V.22, V.22bis, etc." 6:31-36. "In this regard, the fast connect communication protocol is designed to be fast as well as robust, and is accomplished by the use of simple tones." 6:6-11; "However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention	physical layer connection parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated Intrinsic Support: FIGS. 4-7 "Indeed, the significance of the fast connect protocol is achieved when both the calling modem and the answer modem are capable of communicating in accordance with the fast connect modulation protocol herein described so that through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44." (7:23-30.) "Therefore, both the calling and the answer modem can determine that the established communication link is entirely outside the PSTN 34. . . Furthermore, certain assumptions can be made in regard to bandwidth, or transmission quality . . . the calling modem may immediately enter the modem training

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		will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection." 5:53-63; "As will be appreciated by those of ordinary skill in the art, other calling signals may be transmitted by the calling modem. For example, calling signals consistent with that of a facsimile transmission, or calling signals consistent with other modem modulation standards, such as V.34, V.32, V.32bis, etc., may be transmitted." 7:14-19.	and startup sequence 42." (7:67-8:10.) "As will be further appreciated by those of ordinary skill in the art, by making certain assumptions regarding the line quality of the established link, the modem training and startup sequence 42 may be shortened. . . (8:12-23) "As mentioned above, in the training and startup sequence 42 the modems test the established communication link for noise, bandwidth etc. in order to determine the appropriate rate for communication. This is performed using the modulation scheme determined in the automatic mode synchronization sequence 40 as illustrated in FIGS. 4, 5, 6, and 7." (10:63-65). "Consequently, since the call modem knows what type of modem it is and what type of modem the answer modem is, certain shortcuts can be taken during the training and startup sequence 42 so as to reduce the overall connection time. Specifically, the modems can default to preset values that eliminate the need for probing, ranging and half-duplex training. Thus, the modems merely perform a special full-duplex training mode during the training and

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			start-up sequence 42 which results in a much faster connection." (11:2-10.) "Particularly, the probing and ranging sequences are bypassed <u>and the file parameters are assumed</u> in ITU Standard V.8, INFO0, and INFO1. As an example, in ITU Standard V.8, the data call, the LAPM and the full-duplex training parameters are <u>preset to default values</u> if the tones exchanged during automode sequence indicate that both modems are capable of fast connect operation. . .." (11:11-21.) "By choosing a physical layer modulation based on the capabilities of the two modems as determined at run time, the two modems 'negotiate' an appropriate physical layer modulation scheme. *Abbie* on the other hand, *commands* the answer modem to perform a fast connect. There is no negotiation wherein the calling modem accommodates the incapability of the answer modem to carry out a fast connect command. The answer modem simply responds to the calling modem, and there is nothing in *Abbie* to suggest a negotiating system or method. Therefore, *Abbie* fails to teach the feature of having a physical layer connection based on 'a negotiated physical layer modulation.'" (10/28/97 Response at 6 (internal

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			citations omitted) (emphasis in original).) *See also* Cited Prior Art *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.
10. means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer	6(b), 8, 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for establishing a physical layer connection between said calling and said answering modems" Function: Establishing a physical layer connection between the calling and answering modems.	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing a physical layer connection between said calling and said answering modems – *see row 8 above.* physical layer connection -- *see row 6 above*

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connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations		Structure: Control processor programmed to perform the steps of identifying and applying a commonly supported physical layer communication protocol between the calling and answering modems, or the equivalents. (FIG. 2 (40 and 42) and FIG. 9 (114, 124, 120, 124') Intrinsic Support: FIG. 2, 40 and 42; FIG. 9, 114, 124, 120, 124; "To more particularly describe the initial startup sequence in accordance with the modulation standard of the fast connect modem, reference is made to FIGS. 2 and 3. FIG. 2 illustrates the three principal components of modem exchange or communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40. During this period, the modems exchange parameters that identify the modems, and thus, their communication protocol. This sequence 40, thus, synchronizes the modems for communication in accordance with the same	physical layer modulation – *see row 7 above* wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations – *see row 9 above* Structure – calling PSTN or cellular modem having a DSP that listens to and creates frequency tones in accordance with a control processor programmed to perform either the algorithm described in Figure 4 or 6, the control processor including a memory that stores the algorithm; answering PSTN or cellular modem having a DSP that listens to and creates frequency tones in accordance with a control processor programmed to perform either the algorithm described in Figure 5 or 7, the control processor including a memory that stores the algorithm Intrinsic Support: Figures 1, 4-7 and 9 "The use of such simple tone facilitates the implementation of the automatic mode select to be in

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		standard or protocol, such as V.34, V.22, V.22bis, etc." Col. 6, lines 24-56; '631 Patent File History Office Action of September 4, 1997; Response of October 23, 1997.	the modem's control processor rather than the digital signal processor (DSP) chip." (6:6-11.) "The MSC(cellular) modem 20 comprises a digital signal processor (DSP) 112, a control processor 114, and a DTE interface 116. Likewise, the MSC(PSTN) modem 24 comprises a DSP 118, a control processor 120, and a DTE interface 122. . . . . However, each modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. . . . The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." (13:45-14:9.) "[P]resent invention. . . uses different communication techniques (e.g., different frequency

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			tones) to establish the physical and link layer connections <u>since data byte transfer is not yet enabled during the establishment of the physical and link layers</u>." (1/28/98 Response at 7.); *See also* 9/12/97 Rejection; 10/23/97 First Response With Amendments;11/21/97 Office Action (Rejections); 1/28/98 Response to Final Rejection' 4/23/98 Third Response; Cited Prior Art. "Indeed, the significance of the fast connect protocol is achieved when both the calling modem and the answer modem are capable of communicating in accordance with the fast connect modulation protocol herein described so that through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44." (7:23-30.) "Accordingly, at the completion of the automatic mode synchronization sequence 40 (FIG. 2), the modems enter into a training and start-up sequence 42. As mentioned above, in the training and startup sequence 42 the modems test the established communication link for noise, bandwidth, etc., in order to determine the appropriate rate for communication. This is performed using the

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			modulation scheme determined in the automatic mode synchronization sequence 40 as illustrated in FIGS. 4, 5, 6, and 7." (10:57-65.) "For example, in the embodiment described above in Section I, the exchange of tones in the mode synchronization sequence 40 indicates to each modem the type of modem it is communicating with, and therefore, certain assumptions can then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:65-13:4.) "Particularly, the probing and ranging sequences are bypassed and the file parameters are assumed in ITU Standard V.8, INFO0, and INFO1. As an example, in ITU Standard V.8, the data call, the LAPM and the full-duplex training parameters are preset to default values if the tones exchanged during automode sequence indicate that both modems are capable of fast connect operation. . . ." (11:11-21.) V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art

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			See also '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.
11. logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated	10(b)	Rembrandt does not believe this term requires construction. In the alternative: programming that allows a physical layer connection [defined above] between a calling modem [defined above] and an answering modem [defined above] to be applied based on the negotiated physical layer modulation chosen from the first and second physical layer modulations [defined above]. Intrinsic Support: See support for establishing a physical later connection.	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations -- *see row 8 above for construction of this function* Structure – operating code for implementing either the algorithm of Figure 4 or Figure 6

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physical layer modulation chosen from said first and second physical layer modulations		"However, each modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. In the context of the present disclosure, a memory device is a computer readable medium that is embodied in an electronic, magnetic, optical or other physical device or means that can contain or store a computer program, such as the operating code for the modem 20, 24, for use by or in connection with a computer related system or method. The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." 13:58 – 14:10	Intrinsic Support: FIGS. 4-7 "FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem;" (3:40-49.) "The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." (14:1-9.)

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12. establishing said link layer connection based upon said negotiated physical layer	1(c), 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: applying link layer [defined above] parameters for a connection based on the negotiated physical layer modulation. Intrinsic Support:	before the modems can transfer data bytes, the link layer parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems

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modulation		Abstract, FIGS 2-8; "In an effort to facilitate more reliable and platform independent communication links between remotely located computers, communication protocols are typically organized into individual layers or levels comprising a protocol stack. The lowest layer is designed to establish host-to-host communication between the hardware of different hosts. The highest layer, on the other hand, comprises user application programs which pass customer data back and forth across the communication link. Each layer is configured to use the layer beneath it and to provide services to the layer above it. Examples of two protocol stacks are the Opened Systems Interconnect (OSI) seven layer model and the Transmission Control Protocol/Internet Protocol (TCP/IP) five layer model. The OSI seven layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, a session layer, a presentation layer, and an application layer. When combined, the seven layers form a protocol stack that is designed to provide a heterogeneous computer network architecture. The TCP/IP five	communicated Intrinsic Support: "The present invention generally relates to data communication protocols, and more particularly, to presetting the link layer parameters per the physical layer modulation in a protocol stack for modems." (1:17-20.) "The link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection." (Abstract) "Therefore, a heretofore unaddressed need exists in the industry for a system and method that reduces or eliminates the time required to establish a link layer connection so as to minimize the amount of time for establishing a connection between two modems." 2:55-60. "Another step includes establishing a link layer connection based upon the negotiated physical layer modulation This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus,

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		layer model comprises the following layers from lowest to highest: a physical layer, a data link layer, a network layer, a transport layer, and an application layer. Of particular relevance to the present invention is the implementation of the physical layer and data link layer in these systems. The physical layer of the OSI model is the lowest layer and is concerned with establishing the electrical and mechanical connection between two modems. The data link layer is the second lowest layer of the OSI seven layer model and is provided to perform error checking functions as well as retransmitting frames that are not received correctly. As is well known, a variety of standards exist which govern the protocols for communication between modems. For example, V.21, V.22, V.32, V.32bis, V.34, V.42, and V.42bis, are identifiers of differing communication standards recommended by the International Telecommunications Union (ITU). Each one of these is directed to an aspect of either the physical layer or data link layer of the OSI model. The ITU Standard V.34 (hereafter referred to as V.34) is intended for use in establishing a physical layer connection between two remotely located computers over the Public Switch Telecommunications Network (PSTN). The V.34	the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." (3:9-15.) "in accordance with the present invention, set the error-correction parameters to preset values so as to avoid the necessity of negotiating the parameters." 7:48-51 "In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection . . . This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure." (11:46-51.) "Accordingly, the present invention enables an error-corrected connection without having to perform the steps described above with regard to V.42, or those steps associated with other error-correcting protocols as known in the art. The present invention achieves this by presetting the XID phase parameters to

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		standard includes the following primary characteristics: (1) full and half-duplex modes of operation; (2) echo cancellation techniques for channel separation; (3) quadrature amplitude modulation for each channel with synchronous line transmission at selectable symbol rates; (4) synchronous primary channel data signaling rates ranging from 2,400 bits per second to 33,600 bits per second, in 2,400 bit-per-second increments; (5) trellis coding for all data signaling rates; and (6) exchange of rate sequences during start-up to establish the data signaling rate. The features of V.34 are documented in the publicly-available ITU Standard V.34 Specification and are well known by those skilled in the art, and will not be described in detail herein. Another significant feature of V.34, as it relates to the present invention, is the ability to automode to other V.-series modems that are supported by the ITU Standard V.32bis automode procedures. In this regard, V.34 defines signal handshaking that two connecting modems exchange at startup in order to learn the capabilities of the other modem to most efficiently exchange information. While V.34 achieves efficient and generally high speed communication between two communicating	default values that are based upon the negotiated physical layer connection. Therefore, when two multi-mode modems negotiate a physical layer connection, the link layer connection can be immediately established based upon the negotiated physically layer modulation. For example, in the embodiment described above in Section 1, the exchange of tones in the mode synchronization sequence 40 indicates to each modem the type of modem it is communication with, and therefore certain assumptions can then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:59-13:4) "Thus, by establishing the error-correction parameters to default values in accordance with the type of physical error-connection determined by the automode sequence 40, a faster and more reliable connection is established." (13:37-41.) Figs 1-9 *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98

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		modems, it nevertheless possesses several shortcomings that impede even more efficient operation. One significant shortcoming is the lengthy startup sequence which takes approximately 10-15 seconds. Particularly, for cellular customers, the ability to provide faster connections and faster data rates is particularly desirable since the cellular customer typically pays a charge for each cellular call based primarily on the length of the call and several other factors such as day of the week, time of day, roaming, etc. As a result, new fast connect protocols are being developed that provide for faster and more efficient startup operation based upon the system configuration and the path of the established communication link. An example of one such fast connect protocol is Paradyne Corporation's Enhanced Throughput Cellular 2 Quick Connect.TM. (ETC2-QC.TM.). In essence, the ETC2-QC.TM. protocol uses techniques in the physical layer to reduce the physical layer startup time delay to about 1 second." 1:23-2:39; "The present invention overcomes the inadequacies an inefficiencies of the prior art as discussed hereinbefore and well known in the industry. The present invention provides a system and method for	Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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		establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections that comprises the following steps. One step includes establishing a physical layer connection between the calling and the answering modems, wherein the physical layer connection is based on a negotiated physical layer modulation chosen from the first and second physical layer modulations. Another step includes establishing a link layer connection based upon the negotiated physical layer modulation. This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." 2:62-3:15; "FIG. 2 is a diagram illustrating the primary handshaking and data exchange sequences between a calling and an answer modem;	

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		FIG. 3 is a timing diagram similar to FIG. 2, illustrating the signal exchange during the automatic mode synchronization sequence of FIG. 2; FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem; FIG. 8 is a schematic diagram comparing a first connect sequence of two fast connect modems with a conventional link layer connection and a second connect sequence of two fast connect modems with a link layer connection based on the physical layer negotiation in accordance with the present invention; and" 3:34-58; "The following description is divided into two parts. The first part discloses an example of a fast connect protocol for use in a modem system that is suitable	

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		for operating in conjunction with the present invention. It should be noted that the modem system disclosed in the first part is merely illustrative of a system that can benefit from the present invention, as will be evident to those of ordinary skill in the art upon reading the following disclosure. The second part discloses the present invention in the context of the fast connect modem system described in the first part. However, the present invention is equally well suited for application outside the context of the fast connect modem system described herein, for example, with modems that connect slowly." 4:5-18;	
		"By way of illustration, consider a call originated by the computer 15 and cellular modem 16 to the standard PSTN modem 32. The established communication link will pass through the cellular phone 17 to the cell tower 18, through the MSC 12, across link 22 to the MSC(Cellular) modem 20 and to the connected modem 24 via RS-232 connection 38, across link 26 and back through the MSC 12 to the PSTN 34, and ultimately across the two-wire link 36 to modem 32. As will become clear from the description that follows, the cellular modem 16 and the MSC(Cellular) modem 20 will connect and	

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		startup in accordance with the fast connect communication protocol described herein. However, since the established communication link that passes from modem 24 to modem 32 passes through a PSTN 34 and a hybrid converter, then the communication protocol of the present invention will not be adequately supported. Accordingly, the modems 24 and 32 will identify this situation and will connect and communicate using an alternative communication protocol supported by both modems and capable of effective transmission across the established link. In this regard, the overall communication link does not realize the fast connection. Indeed, an aspect of the fast connect protocol described herein is the determination of whether both modems are compatible, in terms of communication protocol, and whether they are connected through a line that passes through a PSTN. If the modems are compatible and the established communication link is outside a PSTN (e.g., cellular to MSC) or is to a PSTN modem with a 4-wire connection that has been configured for supporting a fast connect protocol, then the modems may connect and begin their startup sequence. In this regard, the fast connect communication protocol	

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		is designed to be fast as well as robust, and is accomplished by the use of simple tones. The use of such simple tones facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital signal processor (DSP) chip. In addition to the fast connect protocol discussed in below, the fast connect protocol also includes several "fallback" modulations. More particularly, the modem of the present invention will preferably include Paradyne Corporation's Enhanced Throughput Cellular 1.TM. (ETC1.TM.), V.34, V.32bis, V.32, and V.22bis modulations. Thus, in the previous example, modems 24 and 32 may communicate using one of these communication protocols. These modulation protocols are documented and will be understood by persons of ordinary skill in the art, and will not be discussed herein. It suffices to say that supporting the above-listed modulation standards greatly enhances the flexibility and versatility of a fast connect modem. To more particularly describe the initial startup sequence in accordance with the modulation standard of the fast connect modem, reference is made to FIGS. 2 and 3. FIG. 2 illustrates the three principal components of modem exchange or	

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		communication. After the cellular modem initiates the call, such that a communication link is established, the modems enter a mode select sequence, referred to herein as automatic mode synchronization 40. During this period, the modems exchange parameters that identify the modems, and thus, their communication protocol. This sequence 40, thus, synchronizes the modems for communication in accordance with the same standard or protocol, such as V.34, V.22, V.22bis, etc. Once the modems have synchronized their communication protocol, or modulation standard, then they enter a training and startup sequence 42. In a manner known in the art, during this sequence the modems may test the established communication link for noise, bandwidth, etc., in order to determine an appropriate rate for communication. The modems may also operate during this period to train their internal echo cancellers by, for example, ranging the established link of communication. In accordance with a related aspect of the fast connect modems, under certain circumstances the modem training and startup sequence may also be significantly shortened to provide a more robust (both time-shortened and	

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		reliable) startup sequence. More particularly, the "circumstances" which provide such a robust startup include communicating modems constructed in accordance with the invention detecting an established link of communication that does not pass through any two-wire connections. The completion of this sequence signifies the establishment of a physical layer connection between two modems. After the physical layer has been established, the communicating modems enter the information exchange/communication sequence, referred to herein as error-correction negotiation 44, in order to establish the link layer connection. This is of particular relevance to the present invention in that it includes negotiation of a error-correcting protocol such as V.42. During this sequence 44, the modems detect whether they are error-correcting modems and, if so, they negotiate the error-correcting parameters. Referring now to FIG. 3, the initial automatic mode synchronization 40 is illustrated. As shown, this sequence is executed by exchanging signals between the calling modem and the answer modem. After the calling modem instructs the cellular phone to establish the communication link with the answer	

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		modem, it transmits the calling signal Ciqck 50. As will be described in more detail in connection with the flowcharts of FIGS. 4-7, this signal may comprise a 1900 hertz tone, or alternatively may comprise a 1500 hertz tone modulated with a 1900 hertz tone. If only a 1900 hertz tone is transmitted as Ciqck signal 50, then the answer modem knows that the calling modem is configured as a Central Site, four-wire modem (see FIG. 6). Alternatively, if the CIqck signal includes both 1500 and 1900 hertz components, then the answer modem knows that the calling modem is configured as a cellular modem. As will be appreciated by those of ordinary skill in the art, other calling signals may be transmitted by the calling modem. For example, calling signals consistent with that of a facsimile transmission, or calling signals consistent with other modem modulation standards, such as V.34, V.32, V.32bis, etc., may be transmitted. Since automatic connection and synchronization to facsimile, and these other modulation standards, are well known it will not be discussed herein. Indeed, the significance of the fast connect protocol is achieved when both the calling modem and the answer modem are capable of communicating in accordance with the fast connect modulation	

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		protocol herein described so that through the exchange of tones, the modems are made aware of the possible shortcuts in the fast startup and training sequence 42, and more particularly, in the error-correction negotiation 44. Once the CIqck signal 50 is received by the answer modem, then the answer modem transmits its response back to the calling modem. The purpose of this answer signal is not only to signal receipt of the calling signal, but also to uniquely identify the answer modem. Again, as is known in the art, this answer signal may comprise ANS or ANSam signals as are known by the V.34 and V.32bis communication protocols. If so, the calling modem will then startup and train 42 and perform error-correction negotiation 44. Significant to the present invention, however, is when the answer signal is ANSqck, which is defined by either a 1680 hertz tone or an 800 hertz tone. As illustrated in FIG. 4 (assuming the calling modem is a cellular modem), if ANSqck is an 800 hertz tone, then the calling modem knows that the answer modem is configured as a four-wire connection, and can communicate with the calling modem in accordance with the fast connect communication protocol and, in accordance with the	

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		present invention, set the error-correction parameters to preset values so as to avoid the necessity of negotiating the parameters. In addition, the 800 hertz ANSqck signals the calling modem that the answer modem is connected to a PSTN 34 (see FIG. 1). Therefore, the calling modem transmits a 2100 hertz tone for approximately one second. This, as is known, serves to pad the initial two second connect period, as required by the FCC for billing purposes. Furthermore, it serves to disable the echo cancellers within the PSTN 34. If ANSqck is a 1680 hertz tone, which is the center tone of V.34 S signal, then the calling modem knows that the answer modem is configured as a four-wire connection, and can again communicate with the calling modem in accordance with the fast connect communication protocol and, in accordance with the present invention, set the error-correction parameters to preset values so as to avoid the necessity of negotiating the parameters. More significantly, it tells the cellular calling modem that the answer modem is not connected to the PSTN 34. Therefore, both the calling modem and the answer modem can determine that the established communication link is entirely outside the PSTN 34. Accordingly, the Federal Communications	

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		Commission (FCC) billing delay need not be inserted. Furthermore, certain assumptions may be made in regard to bandwidth, or transmission quality. For example, the established communication link will not pass through echo cancellers, and as a result, the calling modem need not transmit the 2100 hertz tone. Instead, upon receiving the ANSqck answer signal, the calling modem may immediately enter the modem training and startup sequence 42. As will be further appreciated by those of ordinary skill in the art, by making certain assumptions regarding the line quality of the established link, the modem training and startup sequence 42 may be shortened. For example, in the preferred embodiment, the system initiates communication by assuming a 9600 baud rate. It has been found that most cellular connections may transmit at this rate, and certain front-end savings may be realized by defaulting to this initial startup rate. Of course, this rate may be increased, or autorated upwardly, in accordance with methods known in the prior art, after the initial startup and training sequence 42 has been completed. Referring back to FIG. 4, a top-level flowchart is shown, illustrating the automatic mode synchronization of a cellular calling modem	

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		constructed in accordance with the fast connect protocol disclosed herein. Once the calling modem has completed transmitting the dialing sequence, it transmits the CIqck signal, which for a cellular calling modem includes modulated 1500 and 1900 hz tones, as indicated in block 60. Once the calling signal has been transmitted, the calling modem will wait to receive the answer signal from the answer modem. In order to exchange data using the modified modulation standard of the present invention, the calling modem looks to receive one of two answer signals. The first valid answer signal as in 1680 hz tone, which is the center tone of the V.34 S signal, as indicated in block 61. This tone signals to the calling modem that the answer modem is not only compatible to transmit in the fast connect modified modulation standard, but further indicates that the answer modem is connected via four wire connections, and does not interconnect to a PSTN. Accordingly, since the calling modem is a cellular modem, then the established communication link does not pass through a PSTN and the initial two second FCC-required delay need not be inserted into the start-up sequence. Moreover, since the entire communication link is four wire, then the modems need not transmit the 2100 hz signal to disable echo	

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		cancellors. A second valid answer signal is an 800 hz tone, as shown by block 62, which also indicates that the answer modem is connected via four wire, and therefore, can communicate in accordance with the fast connect modulation protocol. In addition, the 800 hz tone indicates that the answer modem is connected to a PSTN. Assuming, as previously discussed, that the requisite steps have been taken to ensure that the established communication link does not pass through a two wire connection, then certain savings or efficiencies can be gained during the modem start-up and training sequences (e.g., eliminate echo training since no hybrid circuits are present in the communication link). Nevertheless, the FCC-required delay must be inserted and, therefore, a 2100 hz tone is transmitted at block 63 by the calling modem for a duration of approximately one second. The amount of the 2100 hz tone will "pad" the total modem automode and startup time to two seconds. This ensures that no customer data is transferred in the first two seconds (which meets FCC requirements). Thereafter, calling modem proceeds with the modem training and start-up sequence at block 64. If neither of the foregoing answer signals are	

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		received, then the system operates to determine whether another valid answer signal has been transmitted from the answer modem. The step of block 65 broadly designates this function. It should be appreciated that well known answer signals such as ANS or ANSam may be transmitted by the answer modem and, if received, the calling modem may synchronize to the appropriate modulation standard, as indicated in block 66. Although not separately designated in the figure, it should be further appreciate that if no valid answer signal is received by the calling modem within a given period of time, the calling modem will time out and abort the attempted communication. Also, and as illustrated at block 67, the calling modem will abort the attempted communication if a busy signal is received. FIG. 5 shows a top-level flowchart illustrating the operation of a cellular answer modem constructed in accordance with the fast connect communication protocol described herein. Once the communication link has been established and the call answered at block 69, the answer modem looks to detect the CIqck calling signal, as indicated by block 70. In the presently described fast connect protocol, cellular to cellular modem communications are not supported.	

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		Therefore, a cellular answer modem will assume that a calling modem transmitted a CIqck signal will transmit only a 1900 hz tone rather than the modulated 1500 and 1900 hz tones. Having said this, it should be appreciated that cellular-to-cellular communications could be supported. In keeping with the description of FIG. 5, once the answer modem has received the CIqck calling signal, it transmits the ANSqck answer signal at block 71. It then waits for the calling modem to enter the modem start-up and training sequence. This sequence is identified by receiving the S signal as assigned by the V.34 modulation standard, as indicated by the decision block 72. Once this signal is received, then the answer modem will transmit back to the calling modem the appropriate S signal, so as to initiate the startup and training sequence 42. Alternatively, if the answer modem, within a period of two seconds, has not received CIqck calling signal, then it will proceed with the start-up sequence in accordance with an alternative modulation standard. This, therefore, assumes that the modified communication protocol of the present invention is not supported by the calling modem, and the answer modem will typically respond to the calling signal of an alternative communication	

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		signal by transmitting a 2100 hz tone, as indicated in block 74. Referring now to FIG. 6, a software flowchart illustrating the top-level operation of a central site calling modem is shown. As depicted, the calling modem originates the call and establishes a communication link at block 80. Once the communication link is established, the calling modem transmits the CIqck calling signal at block 81, which in the case of a central site calling modem comprises a 1900 hz signal tone. If the 1680 hz ANSqck answer signal is detected at block 82, then the calling modem recognizes the answer modem as one capable of transmitting pursuant to the fast connect communication protocol. Thereafter, the calling modem must determine the network configuration of the established communication link, as indicated in block 83. That is, the central site calling modem will determine whether the established communication link passes through a PSTN or not. If it is determined that the established link passes through a PSTN, then, as in the case of the cellular calling modem, the calling modem transmits a 2100 hz signal for approximately one second at block 84. Thereafter, the calling modem enters the modem start-up and training sequence, as	

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		indicated in block 85. Alternatively, if the calling modem detects the ANS answer signal (2100 hz) at block 86, then it communicates with the answer modem using the ETC1.TM. communication protocol and the V.32bis training, as indicated by block 87. If the ANSam answer signal is detected at block 88, then the modem will startup in standard V.34 mode at block 89, which is well known in the art and therefore not described herein. The modem will also monitor for ANSqck at block 82, which in this example is a 1680 Hz tone. If this is not detected, then the modem will startup under an alternate low speed standard at block 90, which is well known in the art and therefore not described herein. If ANSqck is detected, then the modem will operate differently depending on whether it is connected to the PSTN network or not, as indicated by block 83. The modem will know whether it is connected to the PSTN via a configuration option which was set at installation. If connected to the PSTN, then the modem will transmit a 2100 Hz tone for one second at block 84 then proceed to the ETC2.TM. training sequence at block 85. If the modem is not connected to the PSTN at block 83, then it can proceed directly to the ETC2.TM. training sequence at block 85,	

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		avoiding the additional one second of startup shown at block 84. Reference is now made to FIG. 7, which is a software flowchart illustrating the top-level operation of a central site answer modem. As illustrated in the flowchart, and in accordance with the presently disclosed fast connect protocol, when the answer modem is a central-site modem, it assumes that any transmissions made in accordance with the modulation standard with the present invention will be via a communication link with a cellular calling modem. Therefore, block 91 indicates detection the CIqck calling signal in the form of a modulated 1500 and 1900 hz tones, as transmitted by cellular calling modem. If the CIqck calling signal is detected, then the answer modem determines the network configuration at block 92. More specifically, the answer modem determines whether the established communication link passes through a PSTN or not. In the event that the established link does in fact pass through a PSTN, then the answer modem will transmit an 800 hz ANSqck answer signal at block 93. As illustrated in FIG. 4, this instructs the calling modem to transmit the 2100 hz tone. Alternatively, the answer modem will transmit the 1680 hz tone, which instructs the	

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		calling modem to proceed directly with the modem start-up and training sequence at block 94. Thereafter, the answer modem will await transmission of the S signal in accordance with the V.34 start-up sequence, as indicated by block 95. Thereafter, the answer modem will respond by transmitting the S of the V.34 start-up, as indicated by block 96. Since the V.34 start-up sequence is well-known in the art, it would not be described herein. The remainder of the flowchart depicted in FIG. 7 illustrates the central-answer modem operation and connects sequence in accordance with alternative standards that are well-known in the prior art and need not be discussed herein. Accordingly, at the completion of the automatic mode synchronization sequence 40 (FIG. 2), the modems enter into a training and start-up sequence 42. As mentioned above, in the training and startup sequence 42 the modems test the established communication link for noise, bandwidth, etc., in order to determine the appropriate rate for communication. This is performed using the modulation scheme determined in the automatic mode synchronization sequence 40 as illustrated in FIGS. 4, 5, 6, and 7. For purposes of the following	

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		discussion, it is assumed that the call and the answer modems are capable of communicating with one another using a fast connect protocol. Consequently, since the call modem knows what type of modem it is and what type of modem the answer modem is, certain shortcuts can be taken during the training and startup sequence 42 so as to reduce the overall connection time. Specifically, the modems can default to preset values that eliminate the need for probing, ranging and half-duplex training. Thus, the modems merely perform a special full-duplex training mode during the training and start-up sequence 42 which results in a much faster connection. Particularly, the probing and ranging sequences are bypassed and the file parameters are assumed in ITU Standard V.8, INFO0, and INFO1. As an example, in ITU Standard V.8, the data call, the LAPM and the full-duplex training parameters are preset to default values if the tones exchanged during automode sequence indicate that both modems are capable of fast connect operation. Further, in the INFO sequences, the 4 point train, 2800 L symbol rate, the power level drop, and preemphasis filter can also be preset to default values. Thus, the ITU Standard V.8 and INFO	

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		sequences are eliminated. At the completion of the training and start-up sequence 42, the modems have established a physical layer connection and are ready to establish the second layer connection, referred to as the link layer connection, via an error-correction negotiation sequence 44 in accordance with the present invention, as disclosed below." 5:42-11:27; "It is noted, however, that conventional wisdom to date has maintained the link layer connection be independent of the physical layer connection when establishing a connection between two modems. In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection during the automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer connection is established substantially instantaneously upon the completion of the physical layer negotiation. This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure."	

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		11:36-51; "Since automatic connection and synchronization to facsimile, and these other modulation standards, are well known it will not be discussed herein." 7:19-22; "However, the default settings are more often than not undesirable because, for example, most modems wish to negotiate Selective Reject, V.42bis data compression, and longer Frame Lengths and Window Sizes." 12:18-23; "However, each modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. In the context of the present disclosure, a memory device is a computer readable medium that is embodied in an electronic, magnetic, optical or other physical device or means that can contain or store a computer program, such as the operating code for the modem 20, 24, for use by or in connection with a computer related system or method. The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is	

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		used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." 13:58-14:10; "1. A method for establishing a link layer connection between a calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising the steps of: establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and establishing said link layer connection based upon said negotiated physical layer modulation. 2. The method of claim 1, wherein said negotiated physical layer modulation is a fast connect modem modulation.6. A system for establishing a link layer connection between a calling modem having a	

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		plurality of possible first physical layer modulations and a plurality of possible link layer connections and a answering modem having a plurality of possible second physical layer modulations and a plurality of possible second link layer connections, comprising: means for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and means for establishing said link layer connection based upon said negotiated physical layer modulation. 7. The system of claim 6, wherein said negotiated physical layer modulation is a fast connect modem modulation.10. A computer program product having a computer readable medium including computer program logic recorded thereon for use in a calling modem for establishing a link layer convention between said calling modem having a plurality of possible first physical layer modulations and a plurality of possible link layer connections and an answering modem having a plurality of possible second physical layer modulations and a plurality of	

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		possible second link layer connections, comprising: logic for establishing a physical layer connection between said calling and said answering modems, wherein said physical layer connection is based on a negotiated physical layer modulation chosen from said first and second physical layer modulations; and logic for establishing link layer connection based upon said negotiated physical layer modulation." claims 1, 2, 6, 7, 10 '631 Patent File History Office Action of September 4, 1997; Response of October 23, 1997.	
13. means for establishing said link layer connection based upon said negotiated physical layer modulation	6(c), 8, 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for establishing said link layer connection based upon said negotiated physical layer modulation". Function: Establishing a link layer connection based upon a negotiated physical layer modulation. Structure: Control processor programmed to perform the step of establishing link layer	Means plus function element to be construed pursuant to 112, ¶ 6. Function – link layer parameters in the calling and answering modems default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated – *see row 12 above* Structure – control processor in the PSTN or cellular calling modem that operates an algorithm stored in its memory that sets link layer parameters to default

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		parameters to default values that are based upon the previously negotiated physical layer modulation, or the equivalents. (FIG. 2 (44) and FIG. 9 (114, 124, 120, 124') Intrinsic Support: FIG. 2 (44); FIG. 9 (114, 124, 120, 124); "The link layer is the second layer of the ISO model protocol stack and includes negotiating and establishing an error-correcting connection such as with ITU Standard V.42 or Microcom Networking Protocol (MNP). The link layer connection follows the physical layer connection and uses the physical layer in establishing the error-corrected connection. It is noted, however, that conventional wisdom to date has maintained the link layer connection be independent of the physical layer connection when establishing a connection between two modems. In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection during the automatic mode synchronization sequence 40 (FIG. 2). Thus, the steps for establishing an error-correcting protocol are eliminated and the link layer	values that were preset in the calling modem before the modems communicated if a particular physical layer modulation was negotiated; control processor in the answering PSTN or cellular modem that operates an algorithm stored in its memory that sets link layer parameters to default values that were preset in the answering modem before the modems communicated if a particular physical layer modulation was negotiated Intrinsic Support: "[P]resent invention. . . uses different communication techniques (e.g., different frequency tones) to establish the physical and link layer connections since data byte transfer is not yet enabled during the establishment of the physical and link layers." (1/28/98 Response at 7.) *See also* 9/12/97 Rejection; 10/23/97 First Response With Amendments;11/21/97 Office Action (Rejections); 1/28/98 Response to Final Rejection' 4/23/98 Third Response; Cited Prior Art. "The use of such simple tone facilitates the implementation of the automatic mode select to be in the modem's control processor rather than the digital

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		connection is established substantially instantaneously upon the completion of the physical layer negotiation. This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure. By way of example, the ITU Standard V.42 (hereafter referred to as V.42) comprises a detection phase, and exchange identification (XID) phase, and a link establishment phase, all of which are briefly discussed below. A more detailed explanation of V.42 can be found in the publicly-available ITU (CCITT) Recommended Standard V.42 documentation. The detection phase is provided to determine whether the answer modem supports an error-correcting protocol. This phase is designed to avoid the potential disruptions to the answer DTE that could occur if the calling modem immediately enters the XID phase and the answering modem was not capable of an error-correcting communication. However, the detection phase is optional and may be disabled. If the call modem determines that the answering modem does not support a V.42 error-	signal processor (DSP) chip." (6:6-11.) FIGS 1-9 "Accordingly, the present invention enables an error-corrected connection without having to perform the steps described above with regard to V.42, or those steps associated with other error-correcting protocols as known in the art. The present invention achieves this by presetting the XID phase parameters to default values that are based upon the negotiated physical layer connection. Therefore, when two multi-mode modems negotiate a physical layer connection, the link layer connection can be immediately established based upon the negotiated physical layer modulation. For example . .. certain assumption scan then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:55-65.) "The MSC(cellular) modem 20 comprises a digital signal processor (DSP) 112, a control processor 114, and a DTE interface 116. Likewise, the MSC(PSTN) modem 24 comprises a DSP 118, a control processor 120, and a DTE interface 122. . . . . However, each

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
		correcting protocol, there are often times fall-back error protocols provided by the calling modem, such as in the case of V.42, where MNP is provided as a fall-back error-correcting protocol. Alternatively, if the answer modem does not support V.42 nor MNP, then no error-correcting protocol is established and a connect message is issued by the modems to their respective digital terminal equipment so that user data can be transmitted between the two modems. The XID phase is provided for the negotiation of the error-correcting parameter values. These parameters essentially govern the error-correcting operation of the modems once the connection is established. As with the detection phase, the XID phase may be omitted if default parameter values are acceptable. For example, the following are provided as the default parameters values in the V.42 standard: Standard Reject, 16 bit FCS (Frame Check Sequence), V.42bis compression disabled, Frame Length (N401) of 128 octets, and Window Size (k) of 15 frames. However, the default settings are more often than not undesirable because, for example, most modems wish to negotiate Selective Reject, V.42bis data compression, and longer Frame Lengths and Window Sizes. Lastly, the link establishment phase is provided for	modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. . . . The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." (13:45-14:9.) "Another step includes establishing a link layer connection based upon the negotiated physical layer modulation This link layer connection includes parameters that are preset to default values based upon the negotiated physical layer connection. Thus, the modems are able to avoid the link layer negotiation that essentially all other modems perform, thereby providing a faster and more robust connection." (3:9-15.)

U.S. Patent No. 5,852,631	Claims at Issue	REMBRANDT	CABLE PARTIES[1]
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		actually making the error-corrected connection between the two modems. In V.42, this is implemented via a set asynchronous balanced mode extended (SABME) command. The SABME command is used to place the addressed error-corrected entity (i.e., the answering modem) into the connected state. The error-correcting entity then confirms acceptance of the SABME command by the transmission of an unnumbered acknowledgment (UA) response. By acceptance of this command, the error-corrected connection is essentially established and the modems then send a connect message to their respective data terminal equipment, such as computer 15 (FIG. 1)." Col. 11:29-12:35; '631 Patent File History Office Action of September 4, 1997; Response of October 23, 1997.	"in accordance with the present invention, set the error-correction parameters to preset values so as to avoid the necessity of negotiating the parameters." 7:48-51 "In contrast, the present invention establishes the link layer connection based upon the modulation chosen in the physical layer connection . . . This not only reduces the amount of time required to establish a connection between two modems, it makes the connection more robust by removing the necessity of performing additional handshaking that, if corrupted for whatever reason, will result in a disconnect or call connect failure." (11:46-51.) "Accordingly, the present invention enables an error-corrected connection without having to perform the steps described above with regard to V.42, or those steps associated with other error-correcting protocols as known in the art. The present invention achieves this by presetting the XID phase parameters to default values that are based upon the negotiated physical layer connection. Therefore, when two multi-mode modems negotiate a physical layer connection, the link layer connection can be immediately established based upon the negotiated

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
			physically layer modulation. For example, in the embodiment described above in Section 1, the exchange of tones in the mode synchronization sequence 40 indicates to each modem the type of modem it is communication with, and therefore certain assumptions can then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:59-13:4)

"Thus, by establishing the error-correction parameters to default values in accordance with the type of physical error-connection determined by the automode sequence 40, a faster and more reliable connection is established." (13:37-41.)

V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, V.42bis, ETC 1, ETC2, MNP, Provisional Applications, Cited Prior Art

See also '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of |

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
			Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
14. logic for establishing link layer connection based upon said negotiated physical layer modulation	10(c)	Rembrandt does not believe this term requires construction. In the alternative: programming that allows link layer [defined above] parameters for the connection to be applied based on the negotiated physical layer modulation. Intrinsic Support: See support for establishing a link layer connection. "However, each modem is provided with operating code which is stored in a memory device 124, 124' provided with the central processor 114, 120, respectively, though additional memory can also be provided and connected to the control processor 114, 120, if necessary. In the context of the present disclosure, a memory device is a computer readable medium that is embodied in an electronic, magnetic, optical or other physical device or means that can contain or store a computer program, such as the operating code for the modem 20, 24, for use by or in connection with a computer related system or method. The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is	Means plus function element to be construed pursuant to 112, ¶ 6. Function – establishing link layer connection based on said negotiated physical layer modulation – *see row 12 above for construction of this function* Structure – operating code for implementing an algorithm that causes a calling modem to default, based on which physical layer modulation was chosen in the negotiation, to values that were preset in each modem before the modems communicated Intrinsic Support: c"Accordingly, the present invention enables an error-corrected connection without having to perform the steps described above with regard to V.42, or those steps associated with other error-correcting protocols as known in the art. The present invention achieves this by presetting the XID phase parameters to default values that are based upon the negotiated physical layer connection. Therefore, when two multi-mode modems negotiate a physical layer connection, the link layer connection can be

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		used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." 13:58 – 14:10	immediately established based upon the negotiated physical layer modulation. For example . .. certain assumption scan then be made regarding the error-correction negotiation sequence 44 so as to eliminate the steps normally performed to establish an error-corrected connection." (12:55-65.) "The operating code includes control logic that controls, among other things, the type of modulation and error correction techniques utilized which is dependent upon whether the modem is used for cellular or land-line connections. Accordingly, the control processor 114, 120 operates on, or executes, the operating code that is in memory device 124, 124' and configured for implementing the present invention so as to control the operation of modem 20, 24." (14:1-9.) FIGS. 4-7 "FIG. 4 is a software flowchart illustrating the operation of the present invention when the calling modem is a cellular modem; FIG. 5 is a software flowchart illustrating the operation of the present invention when the answer

U.S. Patent No. 5,852,631 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES[1] CONSTRUCTION AND INTRINSIC EVIDENCE
			modem is a cellular modem; FIG. 6 is a software flowchart illustrating the operation of the present invention when the calling modem is a Central-site modem; FIG. 7 is a software flowchart illustrating the operation of the present invention when the answer modem is a Central-site modem;" (3:40-52.) *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability. *See row 13 above*

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U.S. Patent No. 5,710,761 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
1. physical layer of a data connection	1(b), 2, 3, 6, 9(c), 10, 11, 14	Rembrandt does not believe this term requires construction. In the alternative: the parameters of the data connection associated with the physical layer [defined above]. Intrinsic Support: "In establishing a data connection between two modems, the modems perform a 'handshaking' sequence to negotiate various parameters about the data connection, e.g., the type of modulation (which relates to line speed), and the type of error control protocol. The type of modulation is representative of the 'physical' layer of a data connection, while the type of error control protocol is representative of the 'link' layer of the data connection. The negotiation of the physical layer is always negotiated before the link layer." 1:8-16. "FIG. 2 is a flow diagram of an illustrative method embodying the principles of the invention for use in the modem of FIG. 1." 2:62-64 "Turning now to FIG. 2, an illustrative method	ITU V. physical layer industry standard (*e.g.*, V.22, V.22bis, V.32, V.32 bis, V.34) in existence as of May 31, 1995 Intrinsic Support: "The specification is objected to under 37 C.F.R. 1.71 because it fails to provide a date for the associated protocols and standards. <u>A date is important since protocols and standards may change over time</u>." 12/31/96 Office Action "Applicant submits that the applicable date of the cited protocols and standards is the filing date of the present invention. However, Applicant asserts that one skilled in the art would understand that the <u>present invention is applicable to all versions of the **cited** protocols and standards</u>." (4/3/97 Response and Amendment at 4.) "During the physical layer negotiation, modem 100 negotiates the <u>type of modulation</u>, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards." (3:49-51.)

U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
		embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that modem 100 has already initiated a data call to a far-end modem (not shown) and a handshaking sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards." 3:36-51. "In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer." 4:13-15 "Finally, this approach allows a high-speed modem to connect at the highest feasible rate and still negotiate the use of the LAPM protocol." 4:57-59	"The type of modulation is representative of the physical layer of a data connection, while the type of error control is representative of the link layer of the data connection." 1:13-15. "The types of error control protocols used today are: "Link Access Protocol Modem" (LAPM), "Microcom Networking Protocol" (MNP), or "Buffer" (which in reality is no error control)." (1:17-21.) "This type of negotiation sequence typically allows a modem to connect to the widest range of industry-available modems." (1:33-35.) "One way to solve the above-mentioned problem is to have a different negotiation sequence for error control negotiation--"LAPM or Disconnect" for example." (1:59-61.) "However, I have realized a solution that solves all of the above problems and is user friendly. I have observed that almost every high-speed modem (V.34, V.32bis. V.32) has a LAPM mode, and that the LAPM mode is enabled. Further, only the low speed modems (V.22bis or below) are MNP-only or non-

U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
		"In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described." 3:33-37 "The foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope." 4:40-45	error control" (2:13-18.) "When the modem negotiates a V.32 or higher modulation, the modem uses the 'LAPM or Disconnect' error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the 'LAPM, MNP or Buffer' error control sequence." (Abstract; 2:29-34.) "In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection." (2:35-57.) "If the value of the negotiated parameter is greater

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			than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, modem 100 disconnects. On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step 320 as part of the link layer negotiation." (3:55-4:1.) "As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an 'LAPM' protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far- end modem for several seconds using the 'MNP' protocol. If this too is unsuccessful,

U.S. Patent No. 5,710,761 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			modem 100 then falls back to a non-error control mode, i.e., the 'Buffer' mode of operation." (4:4-12.) "In particular, when modem 100 negotiates a V.32 or higher modulation, modem 100 performs step 315, described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above." (4:14-18.) *See*, *e.g.*, abstract, 1:17-24, 1:25-35, 1:35-56, 1:59-2:10; 2:13-24, 2:48-56; 3:49-51; 3:55-58; 3:65-4:4; 4:12-19; 4:31-39 FIGS. 1-2 V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, LAPM, MNP, Buffer *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office

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			Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.
2. to determine a set of parameters for the physical layer of the data connection with the far end data communications equipment	1(b), 2, 3, 6, 9(c), 10, 11, 14	Rembrandt does not believe this term requires construction. In the alternative: to identify a set of parameters to be used for the physical layer [defined above] of the data connection between two data communication devices. Intrinsic Support: "In establishing a data connection between two modems, the modems perform a 'handshaking' sequence to negotiate various parameters about the data connection, e.g., the type of modulation (which relates to line speed), and the type of error control protocol. The type of modulation is representative of the 'physical' layer of a data connection, while the type of error control protocol is representative of the 'link' layer of the data connection. The negotiation of the physical layer is always negotiated before the link layer." 1:8-16. "As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data	before error control, the negotiated physical layer standard is used to determine the physical layer parameters of the data connection Intrinsic Support: "The negotiation of the physical layer is <u>always</u> negotiated before the link layer." (1:15-16.) "And, finally, the modulation (physical layer) is <u>always</u> negotiated before the error-control protocol (link layer)." (2:19-20.) "In particular, as noted above, the negotiation of the line speed (modulation) occurs <u>before</u> the negotiation of the type of error control . . . In other words, even though the line speed was successfully negotiated, the error rate at the line speed is high. This affects the time it takes to perform the <u>subsequent</u> error control negotiation." 1:36-58.

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		connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310." 3:43-52 "In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer." 4:13-15 "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that	"As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connections, as shown in step 305." 3:43-46 FIGS 1-2; abstract. "Furthermore, Sridhar et al. teaches away from present invention by disclosing that the modulation or data rate is selected as a function of the link layer sequence. In fact, Sridhar et al. teach that all the link layer negotiations are performed prior to the negotiation of the physical layer. The Applicant submit that Sridhar et al., teach that direct opposite steps or element functions as defined in the claim as amended." (3/31/97 Response and Amendment at 6.) "In marked contrast, the present invention provides an user friendly apparatus and method to dynamically select the error control negotiation sequence, in the link layer, as a function of a negotiated parameter of the physical layer." (3/31/97 Response and Amendment at 5.) See also '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98

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		modem 100 has already initiated a data call to a far-end modem (not shown) and a handshaking sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link	Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		layer cannot be negotiated, modem 100 disconnects. On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step 320 as part of the link layer negotiation. The software instructions for executing the "LAPM, MNP, or Buffer" error control negotiation sequence are illustratively stored in memory 120 at location 122. As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far-end modem for several seconds using the "MNP" protocol. If this too is unsuccessful, modem 100 then falls back to a non-error control mode, i.e., the "Buffer" mode of operation. In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer. In	

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		particular, when modem 100 negotiates a V.32 or higher modulation, modem 100 performs step 315, described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above. In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below 4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection." 3:33 – 4:30 "In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence.	

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		However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence. In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or	

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		lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence. In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection." 2:27-47 "The present invention relates to data communications equipment, e.g., modems, and, more particularly, to the error control negotiation phase of establishing a data connection." 1:5-6	
3.	error control negotiation sequence[s]	1(c), 2, 3, 6, 9(b),	A sequence of approaches that a communication device may employ concerning transmission errors, wherein the sequence of approaches may include at	a sequence of different types of error control protocols or a disconnection step that the equipment attempts to use in turn, such that when an attempt to

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	10, 11, 14	least one approach that takes no error control action. Intrinsic Support: "The types of error control protocols used today are: "Link Access Protocol Modem" (LAPM), "Microcom Networking Protocol" (MNP), or "Buffer" (which in reality is no error control)." 1:17-20. "In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence. In another embodiment of the invention, a modem	use one such protocol fails, the next option in the sequence is tried Intrinsic Support: "In establishing a data connection between two modems, the modems perform a "handshaking" sequence to negotiate various parameters about the data connection, e.g., the type of modulation (which relates to line speed), and the type of error control protocol. The type of modulation is representative of the "physical" layer of a data connection, while the type of error control protocol is representative of the "link" layer of the data connection. The negotiation of the physical layer is always negotiated before the link layer." (1:8-16.) "The types of error control protocols used today are: 'Link Access Protocol Modem ' (LAPM), 'Microcom Networking Protocol "MNP) or 'Buffer' (which in reality is no error control). Typically, in negotiating the type of error control protocol a modem tries each type of error control protocol in turn. In particular, the modem uses a negotiation sequence defined herein as 'LAPM, MNP, or Buffer.' In this negotiation sequence, the modem attempts to connect

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		uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection." 2:24-47. "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that modem 100 has already initiated a data call to a far-end modem (not shown) and a handshaking	with the far-end modem for several seconds, e.g., 2 seconds, using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, the modem then tries to connect with the far-end modem for several seconds, e.g., 6 seconds, using the "MNP" protocol. If this too is unsuccessful, the modem then falls back to a non-error control mode, i.e., the "Buffer" mode of operation. This type of negotiation sequence typically allows a modem to connect to the widest range of industry-available modems. Unfortunately with higher modulation speeds available, like those in ITU standards V.34 and, to a lesser degree, V.32bis, the above error control negotiation sequence can present a problem. In particular, as noted above, the negotiation of the line speed (modulation) occurs before the negotiation of the type of error control. In order to determine the appropriate line speed, a modem uses a technique called "line probing." Unfortunately, the accuracy of current line probing techniques is not perfect. As a result, a modem may erroneously connect at too high a line speed. In other words, even though the line speed was successfully negotiated, the error rate at

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		sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, modem 100 disconnects." 3:33-64.	that line speed is high. This affects the time it takes to perform the subsequent error control negotiation. In particular, with an increase in the error rate, the LAPM type of error control may not be negotiated within the 2 seconds, mentioned above. Further, in severe cases, the time delay in negotiating the error control protocol will be so long that neither LAPM nor MNP is negotiated, causing the modem to fallback to buffer mode." (1:17-54.) "One way to solve the above-mentioned problem is to have a different negotiation sequence for error control negotiation--"LAPM or Disconnect" for example. With this negotiation setting, the modem tries for an extended length of time, e.g., 30 seconds, to negotiate a LAPM data connection." (1:59-64.) "However, this negotiation sequence presents a problem when connecting to modems that do not support LAPM, i.e., MNP-only or non-error-control modems. In order to connect to MNP-only or non-error-control modems, the user must switch the modem back to using the "LAPM, MNP, or Buffer" error control negotiation sequence, described above. Typically, the user switches between error control negotiation sequences via an respective AT

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		"On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step 320 as part of the link layer negotiation. The software instructions for executing the "LAPM, MNP, or Buffer" error control negotiation sequence are illustratively stored in memory 120 at location 122. As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far-end modem for several seconds using the "MNP" protocol. If this too is unsuccessful, modem 100 then falls back to a non-error control mode, i.e., the "Buffer" mode of operation." 3:65-4:12. "In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer. In particular, when modem 100 negotiates a V.32 or higher modulation, modem 100 performs step 315,	command. This is not user-friendly. In today's marketplace, the configuration of the modem itself, e.g., what type of error control negotiation sequence to use, should be transparent to the user." (1:66-2:10.) "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. . . After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 use an 'LAPM or Disconnect' error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the 'LAPM or Disconnect' error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, the modem 100 disconnects." (3:33-64; Fig. 1; Fig 2)

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		described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above. In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below 4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection." 4:13-4:30. error control negotiation sequences: more than one error control negotiation sequence [defined above]. Intrinsic Support: See support as already defined.	*See also* Abstract. *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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_4._ error control	1(c), 2, 3, 6, 9(b), 10, 11, 14	Any of a variety of approaches employed concerning transmission errors that occur on a communications channel. Intrinsic Support: "The types of error control protocols used today are: "Link Access Protocol Modem" (LAPM), "Microcom Networking Protocol" (MNP), or "Buffer" (which in reality is no error control)." 1:17-20. "In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence.	link layer error control protocol standards (LAPM, MNP, or Buffer) in existence as of May 31, 1995 Intrinsic Support: "The specification is objected to under 37 C.F.R. 1.71 because it fails to provide a date for the associated protocols and standards. A date is important since protocols and standards may change over time." 12/31/96 Office Action "Applicant submits that the applicable date of the cited protocols and standards is the filing date of the present invention. However, Applicant asserts that one skilled in the art would understand that the present invention is applicable to all versions of the **cited** protocols and standards." (4/3/97 Response and Amendment at 4.) "The types of error control protocols used today are: 'Link Access Protocol Modem ' (LAPM), 'Microcom Networking Protocol "MNP) or 'Buffer' (which in reality is no error control). Typically, in negotiating the type of error control protocol a modem tries each type of error control protocol in turn. In particular, the modem uses a negotiation sequence defined

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		In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection." 2:24-47. "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that modem 100 has already initiated a data call to a far-	herein as 'LAPM, MNP, or Buffer.'" (1:17-24.) "I have observed that almost every high-speed modem (V.34, V.32bis, V.32) has a LAPM mode, and that the LAPM mode is enabled. Further, only the low-speed modems (v.22bis or below) are MNP-only or non-error control. . . . In particular, the modem has at least two type (sic) of error control negotiation sequences to select from: 'LAPM or Disconnect,' and 'LAPM, MNP or Buffer.' When the modem negotiates a V.32 or higher modulation, the modem uses the 'LAPM or Disconnect' error control negotiation sequence. However, when the modem negotiates a V.22 bis or lower modulation, the modem uses the 'LAPM, MNP or Buffer' error control sequence." (2:14-34.) FIGS 1-2. V.8, V.21, V.22, V.22bis, V.32, V.32bis, V.34, V.42, LAPM, MNP, Buffer *See also* Abstract, 2:24-48, 3:33-4:11; 4:12-29 *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97

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		end modem (not shown) and a handshaking sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, modem 100	Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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		disconnects." 3:33-64. "On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step 320 as part of the link layer negotiation. The software instructions for executing the "LAPM, MNP, or Buffer" error control negotiation sequence are illustratively stored in memory 120 at location 122. As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far-end modem for several seconds using the "MNP" protocol. If this too is unsuccessful, modem 100 then falls back to a non-error control mode, i.e., the "Buffer" mode of operation." 3:65-4:12. "In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer. In particular, when modem 100 negotiates a V.32 or	

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		higher modulation, modem 100 performs step 315, described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above. In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below 4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection." 4:13-4:30.	
5.	selecting one of a number of error control negotiation sequences as a function of a value of at least	1(c), 2, 3, 6	Rembrandt does not believe this term requires construction. In the alternative: selecting an error control negotiation sequence [defined above] based upon the value of at least one parameter associated with the physical layer [defined above]. Intrinsic Support:	after negotiating the physical layer and determining the physical layer parameters, using the value of at least one determined physical layer parameter to select one of multiple link layer error control negotiation sequences Intrinsic Support:

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one parameter from the set of parameters for the physical layer		See support as already defined. "In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence." 2:24-35 "In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below	"The negotiation of the physical layer is always negotiated before the link layer." (1:15-16.) "And, finally, the modulation (physical layer) is always negotiated before the error-control protocol (link layer)." (2:19-20.) "In particular, as noted above, the negotiation of the line speed (modulation) occurs before the negotiation of the type of error control . . . In other words, even though the line speed was successfully negotiated, the error rate at the line speed is high. This affects the time it takes to perform the subsequent error control negotiation." (1:36-58.) "And, finally, the modulation (physical layer) is always negotiated before the error control protocol (link layer). Therefore, and in accordance with the invention, a modem dynamically selects the type of link layer negotiation sequence as a function of a negotiated parameter of the physical layer." (2:18-23.) "In accordance with the inventive concept, modem 100 dynamically selects the type of error control

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		4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection." 2:36-47 "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described." 3:33-37	negotiation sequence as a function of the type of physical layer negotiated. . . After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 use an 'LAPM or Disconnect' error control negotiation sequence in step 315 as part of the link layer negotiation." (3:33-64.) "On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an 'LAPM, MNP or Buffer' error control negotiation sequence in step 320 as part of the link layer negotiation." (3:65-4:1.) "[T]he present invention provides an user friendly apparatus and method to dynamically select the error control negotiation sequence, in the link layer, as a function of a negotiated parameter of the physical layer. This optimizes the selection of the error control sequence as a result of the selected type of physical layer parameters, which include modulation and data rate." (4/3/97 Response and Amendment at

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			5.) "Furthermore, *Sridhar et al.* teach away from the present invention by disclosing that the modulation or data rate is selected as a function of the link layer sequence. . . . The Applicant submits that *Sridhar et al.*, teach the direct opposite steps or element functions as defined the claims as amended." (4/3/97 Response and Amendment at 5.) *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.
6.	selects from memory one of a number of error control negotiation	9(d), 10, 11, 14	Rembrandt does not believe this term requires construction. In the alternative: Selecting an error control negotiation sequence [defined above] based upon the value of at least one parameter associated with the physical layer [defined above].	after negotiating the physical layer and determining the physical layer parameters, using the value of at least one determined physical layer parameter to select one of multiple link layer error control negotiation sequences

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sequences as a function of a value of at least one parameter from the set of parameters for the physical layer		Intrinsic Support: See support as already defined. "In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence." 2:24-35 "In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below	Intrinsic Support: "The negotiation of the physical layer is always negotiated before the link layer." (1:15-16.) "And, finally, the modulation (physical layer) is always negotiated before the error-control protocol (link layer)." (2:19-20.) "In particular, as noted above, the negotiation of the line speed (modulation) occurs before the negotiation of the type of error control . . . In other words, even though the line speed was successfully negotiated, the error rate at the line speed is high. This affects the time it takes to perform the subsequent error control negotiation." (1:36-58.) "And, finally, the modulation (physical layer) is always negotiated before the error control protocol (link layer). Therefore, and in accordance with the invention, a modem dynamically selects the type of link layer negotiation sequence as a function of a negotiated parameter of the physical layer." (2:18-23.)

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		4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection." 2:36-47 "In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described." 3:33-37	"In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. . . After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 use an 'LAPM or Disconnect' error control negotiation sequence in step 315 as part of the link layer negotiation." (3:33-64.) "On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an 'LAPM, MNP or Buffer' error control negotiation sequence in step 320 as part of the link layer negotiation." (3:65-4:1.) "[T]he present invention provides an user friendly apparatus and method to dynamically select the error control negotiation sequence, in the link layer, as a function of a negotiated parameter of the physical layer. This optimizes the selection of the error control sequence as a result of the selected type of

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			physical layer parameters, which include modulation and data rate." (4/3/97 Response and Amendment at 5.) "Furthermore, *Sridhar et al.* teach away from the present invention by disclosing that the modulation or data rate is selected as a function of the link layer sequence. . . . The Applicant submits that *Sridhar et al.*, teach the direct opposite steps or element functions as defined the claims as amended." (4/3/97 Response and Amendment at 5.) *See also* '631 patent file history at 3/24/97 Amendment; 9/12/97 Office Action; 10/28/97 Amendment; 11/24/97 Office Action; 1/28/98 Response; 2/19/98 Office Action; 4/28/98 Amendment; 6/8/98 Notice of Allowance; 6/30/98 Amendment; 8/18/98 Notice of Entry of Amendment. *See also* '761 patent file history at 12/31/96 Office Action; 4/3/97 Amendment; 7/8/97 Notice of Allowability.

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1. master unit	1(b), 2, 11, 12, 14(a)	Rembrandt does not believe this term requires construction. In the alternative: a data communication device that communicates with one or more modems. Intrinsic Support: FIGS. 1-4, 6-9; "Field of Invention This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." 1:5-10; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor	device installed in a network that sends messages to its remote units using time division multiplexing without packet headers or delimiters Intrinsic Support: "The master unit of the present invention includes . . . . Therefore, the outbound messages from the Krum reference master unit are 'packetized' whereas the instant claimed invention is time division multiplexed without packet headers and delimiters." File History, Sept. 5, 1989 Amendment, p.8.; *see also*, 5/26/89 Office Action; *see also* cited prior art. "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control;" (1:63-65) "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (*see* FIG. II)." (3:18-22)

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		12." 2:56-61; "The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:25-29; "The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the master unit and the preamble which identifies the transmitted remote." 7:15-20.	"Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40." (3:50-52). "The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." (3:52-56). "As part of the installation of this device, both the master and remote units must be initialized." (5:8-9) "From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and traffic data is bit interleaved along with master to remote network timing control and diagnostic information." 6:25-31. FIGS. I-IX
2. remote units communicating	1(c), 2,	Rembrandt does not believe this term requires construction. In the alternative: modems that	configuration where all inbound transmissions to the master unit contain responses to outbound polls to the

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with said master unit in a multidrop configuration	11, 12	communicate with a master unit [defined above] in a network linking multiple units together. Intrinsic Support: FIGS. 1-4, 6-9; "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period." 2:5-10; "This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." 1:5-10; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10	modems that receive time division multiplexed messages without packet headers or delimiters from their master unit Intrinsic Support: "Apparatus and method for time division multiple access in a <u>multidrop system</u> with multiple host applications <u>employing half-duplex polled protocols</u> is disclosed." (Abstract) "This invention relates to an apparatus and method for a master unit in a <u>multidrop network to communicate to and from a plurality of remote units</u>, using a plurality of host applications using half duplex <u>polled</u> protocols, through the use of time division multiple access techniques." (1:7-13) "The present method and apparatus permits multiple <u>multidrop networks</u> (such as Dataphone Digital Service for digital applications or conventional telephone company lines for analog applications), <u>each serving a distinct half-duplex host polled application</u>, to be replaced by a single multidrop network serving each of <u>said</u> host applications." (1:56-62)

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		includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments. Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." 2:56-3:11; "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22	"The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses." (1:63-2:1) "By the use of the foregoing, a user can install several host applications employing half duplex polling on a single multidrop network, without a fundamental limit on the number of applications and without the need for extensive engineering adjustment during the installation and maintenance of the system." (2:27-32) "All remote units (or 'drops') receive messages outbound from the control unit and respond in a unique time period assigned to each host application." (2:5-7) "FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message." (6:11-13) "From the foregoing, it is seen that this system

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		which transmits the data to the various drops or remote units (see FIG. II). The time division multiplexed modulator 22 is typically a baseband modulator for digital applications. The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:20-29; "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40. The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." 3:50-56; "The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the	includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and data traffic is bit interleaved along with master to remote network timing control and diagnostic information." (6:25-32) "7. Upon receiving a poll at the remote DTE, RTS/CTS toggles and the DTE response bits are loaded into a buffer. The remote then transmits these bits in the assigned time slot using the transmit clock reference. Therefore, contention due to inbound poll responses from other remotes is precluded. All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:52-60) "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3) FIGS. I-IX

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		master unit and the preamble which identifies the transmitted remote." 7:15-20.	Intrinsic support - remote unit "The master unit of the present invention includes . . . . Therefore, the outbound messages from the Krum reference master unit are 'packetized' whereas the instant claimed invention is time division multiplexed without packet headers and delimiters." File History, Sept. 5, 1989 Amendment, p.8.; *see also*, 5/26/89 Office Action; *see also* cited prior art. "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control;" (1:63-65) "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (*see* FIG. II)." (3:18-22) "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40." (3:50-52)

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			"The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." (3:52-56) "As part of the installation of this device, both the master and remote units must be initialized." (5:8-9) "From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and traffic data is bit interleaved along with master to remote network timing control and diagnostic information." (6:25-31) FIGS. I-IX
3. communication with a master unit in a multidrop configuration	14(a)	Rembrandt does not believe this term requires construction. In the alternative: modems that communicate with a master unit [defined above] in a network linking multiple units together. Intrinsic Support:	configuration where all inbound transmissions to the master unit contain responses to outbound polls to the modems that receive time division multiplexed messages without packet headers or delimiters from their master unit Intrinsic Support:

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		FIGS. 1-4, 6-9; "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period." 2:5-10; "This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." 1:5-10; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment	"Apparatus and method for time division multiple access in a multidrop system with multiple host applications employing half-duplex polled protocols is disclosed." (Abstract) "This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." (1:7-13) "The present method and apparatus permits multiple multidrop networks (such as Dataphone Digital Service for digital applications or conventional telephone company lines for analog applications), each serving a distinct half-duplex host polled application, to be replaced by a single multidrop network serving each of said host applications." (1:56-62) "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission

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		functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments. Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." 2:56-3:11; "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (see FIG. II). The time division multiplexed modulator 22 is typically a baseband modulator for digital applications.	time; and priority assigned reservation request for long poll responses." (1:63-2:1) "By the use of the foregoing, a user can install several host applications employing half duplex polling on a single multidrop network, without a fundamental limit on the number of applications and without the need for extensive engineering adjustment during the installation and maintenance of the system." (2:27-32) "All remote units (or 'drops') receive messages outbound from the control unit and respond in a unique time period assigned to each host application." (2:5-7) "FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message." (6:11-13) "From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and data traffic is bit interleaved along with master to remote network

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		The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:20-29; "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40. The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." 3: 50-56; "The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the master unit and the preamble which identifies the transmitted remote." 7:15-20.	timing control and diagnostic information." (6:25-32) "7. Upon receiving a poll at the remote DTE, RTS/CTS toggles and the DTE response bits are loaded into a buffer. The remote then transmits these bits in the assigned time slot using the transmit clock reference. Therefore, contention due to inbound poll responses from other remotes is precluded. All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:52-60) "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3) FIGS. I-IX Intrinsic support - remote unit "The master unit of the present invention includes . . . . Therefore, the outbound messages from the Krum

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			reference master unit are 'packetized' whereas the instant claimed invention is time division multiplexed without packet headers and delimiters." File History, Sept. 5, 1989 Amendment, p.8.; *see also*, 5/26/89 Office Action; *see also* cited prior art. "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control;" (1:63-65) "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (*see* FIG. II)." (3:18-22) "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40." (3:50-52) "The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." (3:52-56)

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			"As part of the installation of this device, both the master and remote units must be initialized." (5:8-9) "From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and traffic data is bit interleaved along with master to remote network timing control and diagnostic information." (6:25-31) FIGS. I-IX

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4. application program[s]	1(d), 2, 11, 12, 14(a)	A computer program or process that can be run on a remote communication device, such as a modem. Intrinsic Support: Abstract; FIG. 5; "This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." 1:7-12; "In the prior art, in order to run multiple host applications to multiple modems in a multidrop network, it is common to use a single network channel for each application, thereby effectively resulting in a number of networks rather than a single network. Further, such an arrangement is clearly an inefficient use of leased lines and other equipment." 1:14-25; "It is therefore an object of this invention to provide a method and apparatus for allowing a single multidrop network to run multiple	program that directly meets the needs of a user, such as payroll, inventory control, word processing, accounting, spreadsheet, etc. Intrinsic Support: "By the use of the foregoing, a user can install several host applications employing half duplex polling on a single multidrop network, without a fundamental limit on the number of applications and without the need for extensive engineering adjustment during the installation and maintenance of the system. This allows an **end user** to have fewer modems or data service units/channel service units (DSU/CSU) on the customer premises." (2:27-34)

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		applications to multiple remote units. It is therefore a further object of this invention to provide such a method and apparatus without a fundamental limitation on the number of applications which can be implemented." 1:45-52; "The present method and apparatus permits multiple multidrop networks (such as Dataphone Digital Service for digital applications or conventional telephone company lines for analog applications), each serving a distinct half-duplex host polled application, to be replaced by a single multidrop network serving each of said host applications." 1:56-62; "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period." 2:5-10; "By the use of the foregoing, a user can install several host applications employing half duplex	

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		polling on a single multidrop network, without a fundamental limit on the number of applications and without the need for extensive engineering adjustment during the installation and maintenance of the system. This allows an end user to have fewer modems or data service units/channel service units (DSU/CSU) on the customer premises." 2:26-34; "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." 4:53-61; "The master unit sends a message to one of the remote units. An inbound message is received from one of the remote units. The address, cyclic redundancy calculation (i.e. checksum) and priority level are checked. If any of these values are invalid, the master unit retransmits to the remote unit. If	

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		these values are valid and there is no reservation request, the message is output to the appropriate application host port at the master end. This process is continually repeated for each application in each remote unit." 5:59-68; "The master unit preassigns time slots within the subframes, one for each of the independent host applications." 6:49-51.	
5. in a time slot assigned to each of said application programs	1(d), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: in one of the time slots assigned to the application programs [defined above]. Intrinsic Support: FIGS. 1-4, 6-9. "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period." 2:5-10;	each application program is assigned to a single time slot per subframe Intrinsic Support: "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61) "6. The master unit preassigns time slots within the

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		"Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments. Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." 2:68-3:11; "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages.	subframes, one for each of the independent host applications." (6:49-51) "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3) FIGS. V, VI-IX "Host applications can request extra time slots for long messages via a request bit within the message format." (Abstract) "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all

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		FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits." 4:53-66; "The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." 5:14-23; "Finally, "set-up" parameters are transmitted from the master unit to the remote units so as to establish remote unit transmit clock advances, priority level, and inbound time slot assignments for the primary and diagnostic channels. The remote unit verifies receipt to the master unit.	of the information from the remote units and allow for control format messages. All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." (1:63-2:19). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-27)

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		Initialization of the remote drops is disclosed in FIG. VII. The user inputs the address of the drop or remote unit. The remote unit returns or "loops-back" the ranging signal from the master unit. The remote unit receives the frame period, the number of time slots per subframe, inbound message lengths, port speed and inbound burst (digital) or transmission (analog) rate. The remote unit receives set-up parameters such as clock advance, priority level and inbound time slot assignment for the primary and diagnostic framing and set-up information to the master unit." 5:40-56; "The master unit preassigns time slots within the subframes, one for each of the independent host applications. 7. Upon receiving a poll at the remote DTE, RTS/CTS toggles and the DTE response bits are loaded into a buffer. The remote then transmits these bits in the assigned time slot using the transmit clock reference. Therefore, contention due to inbound poll responses from other remotes is precluded." 6:49-57;	10/18/89 Office Action; 2/13/90 Response ("In response to the Examiner's rejection regarding the antecedent basis for 'said time slots', Claim 1 has been amended." (p.5)

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		"The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units. Each of these outbound transmissions are error protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:66-7:14.	
6. said time slots	1(e)	said intervals of time. Intrinsic support:	each application program is assigned to a single time slot per subframe Intrinsic Support:

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		See cited support above for the term "in a time slot assigned to each of said application programs" and the support cited below for the term "time slot assigned to each of said application programs."	"The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61) "6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51) "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3) FIGS. V, VI-IX "Host applications can request extra time slots for long messages via a request bit within the message format."

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			(Abstract) "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. <u>All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application.</u> Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system

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			efficiency." (1:63-2:19). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-27) 10/18/89 Office Action; 2/13/90 Response ("In response to the Examiner's rejection regarding the antecedent basis for 'said time slots', Claim 1 has been amended." (p.5)
7. time slot assigned to each of said application programs	1	An interval of time during which data from an application program may be transmitted. Intrinsic Support: "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is	each application program is assigned to a single time slot per subframe Intrinsic Support: "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is

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		thereby avoided due to the fact that each application is assigned such a unique time period." 2:5-10;

"Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments.

Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12.

The aggregate rate multiplexing module 16, in response to commands from the network timing and control processor 12, sets up the timing and bit interleaving of the various application inputs from the various input ports of the primary channel multiplexer 18 and of the overhead and control bits required for outbound control of the remote units from the ranging and network initialization | further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61)

"6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51)

"9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3)

FIGS. V, VI-IX

"Host applications can request extra time slots for long messages via a request bit within the message format." (Abstract)

"The basic features of this method and apparatus are time division multiplexed outbound transmissions |

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		generator 20." 2:68-3:16; "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages. FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits." 4:53-66; "The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate	from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." (1:63-2:19). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its

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		individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." 5:14-23; "Finally, "set-up" parameters are transmitted from the master unit to the remote units so as to establish remote unit transmit clock advances, priority level, and inbound time slot assignments for the primary and diagnostic channels. The remote unit verifies receipt to the master unit. Initialization of the remote drops is disclosed in FIG. VII. The user inputs the address of the drop or remote unit. The remote unit returns or "loops-back" the ranging signal from the master unit. The remote unit receives the frame period, the number of time slots per subframe, inbound message lengths, port speed and inbound burst (digital) or transmission (analog) rate. The remote unit receives set-up parameters such as clock advance, priority level and inbound time slot assignment for the primary and diagnostic framing and set-up information to the master unit." 5:40-56;	message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-27) 10/18/89 Office Action; 2/13/90 Response ("In response to the Examiner's rejection regarding the antecedent basis for 'said time slots', Claim 1 has been amended." (p.5)

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		"The master unit preassigns time slots within the subframes, one for each of the independent host applications. 7. Upon receiving a poll at the remote DTE, RTS/CTS toggles and the DTE response bits are loaded into a buffer. The remote then transmits these bits in the assigned time slot using the transmit clock reference." 6:49-56	
8. messages outbound from said master unit	1(d), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: the remote units get messages from the master unit [defined above]. Intrinsic Support: FIGS. 1-4, 6-9; 1:5-10; "All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period."	messages sent from the master unit to remote units using time division multiplexing without packet headers or delimiters Intrinsic Support: "The master unit of the present invention includes . . . . Therefore, the outbound messages from the Krum reference master unit are 'packetized' whereas the instant claimed invention is time division multiplexed without packet headers and delimiters." File History, Sept. 5, 1989 Amendment, p.8.; see also, 5/26/89 Office Action "The basic features of this method and apparatus are time division multiplexed outbound transmissions

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		2:5-10; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments. Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor	from the master to the remote units for data and control;" (1:63-65). "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (*see* FIG. II)." (3:18-22). "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40." (3:50-52). "As part of the installation of this device, both the master and remote units must be initialized." (5:8-9). "From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and traffic data is bit interleaved along with master to remote network timing control and diagnostic information." (6:25-31). FIGS. I-IX

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		14 communicates such a granted request to the network timing and control processor 12." 2:56-3:11; "The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (see FIG. II). The time division multiplexed modulator 22 is typically a baseband modulator for digital applications. The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:20-29; "Referring now to FIG. II, data outbound from the time division multiplexed modulator 22 of FIG. I is received by the demodulator 38 of remote unit 40. The output of demodulator 38 is demultiplexed by demultiplexer 42 which, in turn, feeds the primary data receiver ports and any diagnostic or secondary channel required by the particular application." 3:50-56;	

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		"10. The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the master unit and the preamble which identifies the transmitted remote." 7:15-20.	
9. master network timing means	1(e), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: a process or device, such as a network timing control processor, that provides timing for the master unit [defined above]. Intrinsic Support: Claim 10; FIGS. 1 & 3, element 12; "Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations,	network timing and control processor that stores user-input initialization parameters including network clock framing periods, slot and subframe assignments. This is a "coined term" defined by the patent. Alternatively, if construed under Section 112, ¶6, it has this construction as its corresponding structure. Intrinsic Support: "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict

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		arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." 2:60-3:6; "This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." 5:15-24; "2. The master unit periodically transmits a network clock reading to all remotes and performs a roundtrip delay transmission calculation ("ranging") to each remote unit. The master unit	functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each 'drop' or remote unit, priority assignments, drop addressing, and port speed assignments." (2:57-3:6). "As part of the installation of this device, both the master and remote units must be in initialized. As is disclosed in FIG. VI, the first step in the initialization of the master unit is to input the directory of users. This is an address entry for each host application drop. The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed

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		informs each remote unit of its precise round trip value. 3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote. 4. The remote establishes a receive clock reference (a delayed version of the Master Network Clock) and a transmit clock reference." 6:32-42; claim 3; FIGS. 1-4, 6-9	assignments. This information is stored in the network timing and control processor." (5:10-24). FIGS I & III ("USER INITIALIZATION"); VI. "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61). "6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51). "Initialization of the remote drops is disclosed in FIG. VII. The user inputs . . . The remote unit returns of 'loops-back' the ranging signal from the master unit. (5:45-52)
<u>10.</u> a period which is divided into	1(e), 2,	Rembrandt does not believe this term requires construction. In the alternative: with a time period	during initialization, a fixed, repeating length of time called a frame is divided by a user into subframes,

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a plurality of subframes, wherein each subframe is divided into said time slots, and each of said time slots is used as an interval in which one of said application programs in said one of said remote units is assigned to transmit	11, 12	used by the master unit, the time period being logically divided into subframes [defined below], each of which being further divided into time slots, and where each time slot is assigned to an application program [defined above] associated with a remote unit as a time period within which that application program [defined above] may transmit.

Intrinsic Support:

"Network initialization parameter extraction module 44 and timing and control block 46 provide the user with network timing extraction information, the slot assignment in which the user is allowed to operate and any control information such as transmit inhibit, transmit enable, reservation grants and other network control provided by the master unit (see FIG. I)." 3:59-65;

"The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a | each of which is divided into the same number of time slots, where each time slot in a subframe is assigned by a user to a different application, whereby the subframes and time slot assignments repeat from frame to frame

Intrinsic Support:

FIG. V

"All remote units (or 'drops') receive messages outbound from the control unit and respond in a unique time period assigned to each host application." (2:5-7).

"Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." (2:68-3:6).

"The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is |

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		preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." 4:53-61;	further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61).
		"As is disclosed in FIG. VI, the first step in the initialization of the master unit is to input the directory of users. This is an address entry for each host application drop.	"FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time." (4:62-64).
		The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." 5:10-23;	"The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." (5:14-23).
		"6. The master unit preassigns time slots within the subframes, one for each of the independent host applications.	"Initialization of the remote drops is disclosed in FIG. VII. The user inputs . . . The remote unit returns of 'loops-back' the ranging signal from the master unit.

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		7. Upon receiving a poll at the remote DTE, RTS/CTS toggles and the DTE response bits are loaded into a buffer. The remote then transmits these bits in the assigned time slot using the transmit clock reference. Therefore, contention due to inbound poll responses from other remotes is precluded. All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits. In the case of analog networks, the preamble is unique to the remote and enables the master to rapidly set the equalization taps and automatic gain control. 8. All inbound transmissions are at burst rates exceeding the remote port rate. 9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for	(5:45-52) FIG. VI. "3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote." (6:37-39). "6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51).

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		error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units. Each of these outbound transmissions are error protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:49-57; "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units. Each of these outbound transmissions are error	

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		protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:66-7:14; " If these values are valid, the message is output to the host port. If the values are not valid, the initial step of an outbound transmission from the master to the remote is returned. FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data,	

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		reservation request, priority level, delimiter and CRC bits. From the foregoing, it is seen that this system includes the following features: 1. The master to remote (outbound) transmission is a constant carrier time division multiplexed bit stream in which multiple Host/FEP poll and data traffic is bit interleaved along with master to remote network timing control and diagnostic information. 2. The master unit periodically transmits a network clock reading to all remotes and performs a roundtrip delay transmission calculation ("ranging") to each remote unit. The master unit informs each remote unit of its precise round trip value. 3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote. 4. The remote establishes a receive clock reference (a delayed version of the Master Network Clock)	

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		and a transmit clock reference. 5. For analog applications, the remote sends a long train to the master and the master trains and stores equalization taps and automatic gain control settings unique to the drop. This is unnecessary for digital networks due to the continuous presence of traffic (either idle codes or data). 6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." 6:7-51	
11. dividing a period of a clock in said master unit into a number of subframes dividing each subframe into a number of slots, each corresponding to transmission times for one	14(c)	Rembrandt does not believe this term requires construction. In the alternative: a time period used by the master unit being logically divided into subframes [defined above], each of which being further divided into time slots, and where each time slot is assigned to an application program [defined above] associated with a remote unit as a time period within which that application program [defined above] may transmit. Intrinsic Support: See claim1 above.	during initialization, a fixed, repeating length of time called a frame is divided by a user into subframes, each of which is divided into the same number of time slots, where each time slot in a subframe is assigned by a user to a different application, whereby the subframes and time slot assignments repeat from frame to frame Intrinsic Support: FIG. V "All remote units (or 'drops') receive messages

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of said remote units and assigning a slot to each of said application programs in said one of said remote units		claim 15; FIGS. 1-4, 6-9.	outbound from the control unit and respond in a unique time period assigned to each host application." (2:5-7). "Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." (2:68-3:6). "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61). "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time." (4:62-64). "The next step is to input the address priority level.

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			This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." (5:14-23). "Initialization of the remote drops is disclosed in FIG. VII. The user inputs . . . The remote unit returns of 'loops-back' the ranging signal from the master unit. (5:45-52) FIG. VI. "3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote." (6:37-39). "6. The master unit preassigns time slots within the subframes, one for each of the independent host

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			applications." (6:49-51).
12. subframe[s]	1(e), 2, 11, 12, 14	Rembrandt does not believe this term requires construction. In the alternative: a portion of a time period. Intrinsic Support: FIG. 5; "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages. FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits. The reservation and priority bits may	division of a frame that contains a fixed number of time slots that must begin and end within the frame, assigned by a user to a single remote unit Intrinsic Support: FIGS. V-VII "Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." (2:68-3:6). "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a

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		be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc. Due to the number of total bits exceeding the number of message bits, the aggregate burst (in the case of analog) or transmission (in the case of digital) rate must be higher than the sum of the independent port rates." 4:53-5:7; " This frame is further segmented into subframes at the remote." 6:38-40	reservation request for longer messages." (4:53-61). "3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote." (6:37-39).
13. each corresponding to transmission times for one of said remote units.	14(c)	Rembrandt does not believe this term requires construction. In the alternative: each time slot is a transmission time for one of the remote units. Intrinsic Support: Abstract; FIGS 1 & 3, elements 12, 20, 32; "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units	"each" refers to each subframe division of a frame that contains a fixed number of time slots that must begin and end within the frame, assigned by a user to a single remote unit Intrinsic Support: FIGS. V-VII

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		for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." 1:63-2:17; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the	"Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." (2:68-3:6). "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61). "3. The period of the master network clock transmission establishes a "frame". This frame is further segmented into subframes at the remote." (6:37-39).

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		several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments.´2:57-3:6; "The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:25-29;	

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		"The ranging receiver 32 receives data from the demodulator 28 during an initial training period (to be described later) so as to store round trip transmission times to each remote unit. This allows an optimization in synchronization of the time division multiple access process, thereby reducing "guard time" between the reception of data from the various remote units thereby increasing the total data transfer rate of the system." 3:42-49; "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits. The reservation and priority bits may be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc." 4:62-5:3; "The initialization phase of operation also includes a ranging calculation for each combination of remote unit (or "drop") and application. The master unit sends a message which makes a round-trip	

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		between the master unit and the individual remote unit. The delay period is stored in a library table in the network timing and control processor 12 so that the remote to master unit communication is synchronized, thereby reducing guard time required between successive transmissions and increasing the efficiency of the system." 5:24-34; "2. The master unit periodically transmits a network clock reading to all remotes and performs a roundtrip delay transmission calculation ("ranging") to each remote unit. The master unit informs each remote unit of its precise round trip value." 6:32-36; FIGS. 1-4, 6-9; "BACKGROUND OF INVENTION 1. Field of Invention This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of	

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		time division multiple access techniques." 1:5-10; "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12." 2:56-61; "The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:25-29; "10. The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the master unit and the preamble which identifies the transmitted remote." 7:15-20.	

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14. ranging means	1(f), 2, 11, 12	Rembrandt does not believe this term requires construction. In the alternative: a device or process that communicates with the master network timing means [defined above] that determines the transmission times between the master unit [defined above] and each of the remote units and sends each of the respective remote units [defined above] the corresponding transmission time between the master unit and that remote unit. Intrinsic Support: Abstract; FIGS 1 & 3, elements 12, 20, 32; "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. All remote units (or	Means plus function element to be construed pursuant to 112, ¶ 6. Function – communicating with said master network timing means wherein a transmission time between said master unit and each of said respective remote units is calculated and transmitted from said master unit to each of said respective remote units, each of said respective remote units using said transmission time to adjust initiation of said time slots. Structure – network timing and control processor **12** (including library table), the ranging and network initialization generator **20**, and ranging receiver **32**, executing an algorithm to perform, during initialization of the master unit before the remote units transmit data, a ranging calculation for each combination of remote unit and application Intrinsic Support: FIGS I-III; VI-VII. "The initialization phase of operation also includes a ranging calculation for each combination of remote unit (or "drop") and application. The master unit sends

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		"drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." 1:63-2:17; "The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:25-29; "The ranging receiver 32 receives data from the demodulator 28 during an initial training period (to be described later) so as to store round trip transmission times to each remote unit. This allows	a message which makes a round-trip between the master unit and the individual remote unit. The delay period is stored in a library table in the network timing and control processor 12 so that the remote to master unit communication is synchronized, thereby reducing guard time required between successive transmissions and increasing the efficiency of the system." (5:24-34). "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters. Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each 'drop' or remote unit, priority assignments, drop

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		an optimization in synchronization of the time division multiple access process, thereby reducing "guard time" between the reception of data from the various remote units thereby increasing the total data transfer rate of the system." 3:42-49; "Additionally, the ranging calculations, that is, the master unit calculation of the time a signal takes to go from the master unit to any remote unit and vice versa, is stored in the timing and control block 46 where it is used for time advancing the transmit clock." 3:65-4:2; "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits. The reservation and priority bits may be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc." 4:62-5:3; "The master unit sends a message which makes a	addressing, and port speed assignments." (2:57-3:6). "The aggregate rate multiplexing module 16, in response to commands from the network timing and control processor 12, sets up the timing and bit interleaving of the various application inputs from the various input ports of the primary channel multiplexer 18 and of the overhead and control bits required for outbound control of the remote units from the ranging and network initialization generator 20. The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (see FIG. II). The time division multiplexed modulator 22 is typically a baseband modulator for digital applications." (3:12-24). "Demodulator 28 provides digital data to the expansion buffers 30, the ranging receiver 32, the reservation request processor 14 and the bit/baud timing processor 34." (3:35-38). "The ranging receiver 32 receives data from the demodulator 28 during an initial training period (to be described later) so as to store round trip transmission times to each remote unit. This allows an optimization

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		round-trip between the master unit and the individual remote unit. The delay period is stored in a library table in the network timing and control processor 12 so that the remote to master unit communication is synchronized, thereby reducing guard time required between successive transmissions and increasing the efficiency of the system." 5:26-34; "2. The master unit periodically transmits a network clock reading to all remotes and performs a roundtrip delay transmission calculation ("ranging") to each remote unit. The master unit informs each remote unit of its precise round trip value." 6:32-36	in synchronization of the time division multiple access process, thereby reducing "guard time" between the reception of data from the various remote units thereby increasing the total data transfer rate of the system." (3:42-49). FIG. II "Additionally, the ranging calculations, that is, the master unit calculation of the time a signal takes to go from the master unit to any remote unit and vice versa, is stored in the timing and control block 46 where it is used for time advancing the transmit clock." (3:65-4:2). "Initialization of the remote drops is disclosed in FIG. VII. The user inputs . . . The remote unit returns of 'loops-back' the ranging signal from the master unit. 5:45-52 "The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock." 6:17-22.

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15. reservation request generator	2	A device or process that adds to a message a request for additional time slots. Intrinsic Support: FIGS. 2, 4, 9 element 54; "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses." 1:63-2:1; "In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." 2:18-26;	component in the remote unit that monitors a compression buffer for fields exceeding a preset parameter limit stored in the initialization parameter table, senses whether an application sending a message requires more than its one subframe time slot, and activates the reservation request bit in its time slot to request use of time slots assigned to subsequent remote units for the remainder of the message Intrinsic Support: "The Applicant has amended Claim 14 in accordance with the Examiner's observation that 'bits' should read 'bit'." (File History, March 5, 1990 Amendment, p.6). "All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:57-60). "In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use

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		"The timing and control block 46 supplies control bits to compression buffers 48. The timing and control block 46 also feeds the preamble and cyclic redundancy check ("checksum") module 50 and the modulator 52. Additionally, the timing and control block 46 sets up the reservation request generator 54. Reservation request generator 54 monitors the compression buffer for fields exceeding a preset parameter limit which is stored in the initialization parameter table. If a field length exceeding the parameter is sensed, then reservation request generator 54 automatically sets the reservation bits in the outgoing message." 4:3-14; "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." 4:53-61;	the time division multiple access slots of subsequent units." (2:18-26). "Additionally, the timing and control block 46 sets up the reservation request generator 54. Reservation request generator 54 monitors the compression buffer for fields exceeding a preset parameter limit which is stored in the initialization parameter table. If a field length exceeding the parameter is sensed, then reservation request generator 54 automatically sets the reservation bits in the outgoing message. The format of the outgoing message, including reservation bits, crc bits, message traffic and preambles are described later herein." (4:6-16). "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits. The reservation and priority bits may be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc." (4:62-5:3).

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"The master unit sends a message to one of the remote units. An inbound message is received from one of the remote units. The address, cyclic redundancy calculation (i.e. checksum) and priority level are checked. If any of these values are invalid, the master unit retransmits to the remote unit. If these values are valid and there is no reservation request, the message is output to the appropriate application host port at the master end. This process is continually repeated for each application in each remote unit. If the aforementioned values are valid but there is a reservation request, then the message is queued in the event that there is a higher priority request or acknowledged and completely received in the event that there is no higher priority request. After the complete message is received, its address, checksum and priority are validated. If these values are valid, the message is output to the host port. If the values are not valid, the initial step of an outbound transmission from the master to the remote is returned. FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a	"FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." (6:11-24). "If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units." (7:7-9). "During this period the expansion buffer clocks data bits to the host." (7:13-14). FIG. I, II, V, VIII; IX

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		DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." 5:59-6:24; "The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit"	

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		command to all of the other remote units. Each of these outbound transmissions are error protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:66-7:14.	
16.	reservation request bit	2, 11	Rembrandt does not believe this term requires construction. In the alternative: at least one bit in a message in order to indicate to the master unit [defined above] that the remote unit [defined above] wants additional time to be allocated to it for a message.

Intrinsic Support:

See support cited above for the term "reservation request generator" | bit contained in each time slot in which a remote unit may transmit that allows the remote unit to request temporary use of preassigned time slots of subsequent remote units

Intrinsic Support:

"The Applicant has amended Claim 14 in accordance with the Examiner's observation that 'bits' should read 'bit'." (File History, March 5, 1990 Amendment, p.6).

"All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:57-60).

"In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit |

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			can append a request for additional time onto its message to the master unit." (2:18-22). "Reservation request processor 14 allows a drop or remote unit to <u>request more than a single time slot</u> for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." (3:7-11). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. <u>The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units.</u>" (2:18-27). "Additionally, the timing and control block 46 sets up the reservation request generator 54. Reservation request generator 54 monitors the compression buffer for fields exceeding a preset parameter limit which is stored in the initialization parameter table. If a field length exceeding the parameter is sensed, then reservation request generator 54 automatically sets the

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			reservation bits in the outgoing message. The format of the outgoing message, including reservation bits, crc bits, message traffic and preambles are described later herein." (4:6-16). "FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." (6:11-24). "The master unit clocks the received message bits to expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an 'authorization to transmit' command and transmits a 'transmit inhibit' command to all of the other remote units. The

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			authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." (7:4-13). FIG. I, II, V, VIII; IX
17. reservation request generator which activates a reservation request bit for requesting an additional time interval inbound to said master unit	2, 11	Rembrandt does not believe this term requires construction. In the alternative: a reservation request generator [defined above] in a remote unit that sets at least one bit in a message in order to indicate to the master unit [defined above] that the remote unit [defined above] wants additional time to be allocated to it for a message. Intrinsic Support: See support cited above for the term "reservation request generator."	component in the remote unit that monitors a compression buffer for fields exceeding a preset parameter limit stored in the initialization parameter table, senses whether an application sending a message requires more than its one subframe time slot, and activates the reservation request bit in its time slot to request use of time slots assigned to subsequent remote units for the remainder of the message Intrinsic Support: "The Applicant has amended Claim 14 in accordance with the Examiner's observation that 'bits' should read 'bit'." (File History, March 5, 1990 Amendment, p.6). "All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:57-60).

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			"In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-26). "Additionally, the timing and control block 46 sets up the reservation request generator 54. Reservation request generator 54 monitors the compression buffer for fields exceeding a preset parameter limit which is stored in the initialization parameter table. If a field length exceeding the parameter is sensed, then reservation request generator 54 automatically sets the reservation bits in the outgoing message. The format of the outgoing message, including reservation bits, crc bits, message traffic and preambles are described later herein." (4:6-16). "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error

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			detection bits. The reservation and priority bits may be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc." (4:62-5:3). "FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." (6:11-24). "If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of

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			the other remote units." (7:7-9). "During this period the expansion buffer clocks data bits to the host." (7:13-14). FIG. I, II, V, VIII; IX

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18. reservation request processor	2	A device or process for receiving and processing requests for additional time slots from a reservation request generator. Intrinsic Support: FIGS. 1, 3, 8 element 14; "In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." 2:18-26; "Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." 3:7-11; "The time division multiple access sequence is established by the user. An epoch period or frame	a processor communicating to said master network timing means to allow a remote unit to request temporary use of preassigned time slots of subsequent remote units for transmitting messages that are longer than a single slot [*See row 19 below* for construction of the complete and actual claim term at-issue:: "reservation request processor communicating to said master network timing means, said reservation request processor being responsive to said reservation request bit"] Intrinsic Support: "Reservation request processor 14 allows a drop or remote unit to <u>request more than a single time slot</u> for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." (3:7-11). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. <u>The master unit will then</u>

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		is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, one for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." 4:53-61; "The master unit sends a message to one of the remote units. An inbound message is received from one of the remote units. The address, cyclic redundancy calculation (i.e. checksum) and priority level are checked. If any of these values are invalid, the master unit retransmits to the remote unit. If these values are valid and there is no reservation request, the message is output to the appropriate application host port at the master end. This process is continually repeated for each application in each remote unit." 5:59-6:10; "The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define	compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-27). "The time division multiple access sequence is established by the user. An epoch period or frame is defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61). "6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51). "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response

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		the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units. Each of these outbound transmissions are error protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:66-7:14	delays." (6:66-7:3). "Host applications can request extra time slots for long messages via a request bit within the message format." (Abstract). "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division

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			multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." (1:63-2:19). "The master unit clocks the received message bits to expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an 'authorization to transmit' command and transmits a 'transmit inhibit' command to all of the other remote units. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." (7:4-13). FIG. I, II, V, VIII; IX said master network timing means – *see row 9 above*

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19. reservation request processor communicating to said master network timing means, said reservation request processor being responsive to said reservation request bit	2, 11	Rembrandt does not believe this term requires construction. In the alternative: a reservation request processor [defined above] communicating with the master network timing means [defined above] to process requests from remote units for additional time slots communicated from the remote units to the reservation request processor using reservation request bits. Intrinsic Support: See above for reservation request processor.	a processor communicating to said master network timing means to allow a remote unit to request temporary use of preassigned time slots of subsequent remote units for transmitting messages that are longer than a single slot Intrinsic Support: "Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." (3:7-11). "In order to accommodate longer messages lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-27). "The time division multiple access sequence is established by the user. An epoch period or frame is

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			defined by the user. The frame is divided with respect to time into a number of subframes. The subframe is further subdivided into slots, **one** for each application. Therefore, an application has a preassigned time period (or slot) within a subframe to transmit from the remote unit to the master unit, with the possibility of a reservation request for longer messages." (4:53-61). "6. The master unit preassigns time slots within the subframes, one for each of the independent host applications." (6:49-51). "9. The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:66-7:3). "Host applications can request extra time slots for long messages via a request bit within the message format." (Abstract). "The basic features of this method and apparatus are time division multiplexed outbound transmissions

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			from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for control format messages. <u>All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application.</u> Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." (1:63-2:19). "The master unit clocks the received message bits to expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the

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			master responds to the remote with an 'authorization to transmit' command and transmits a 'transmit inhibit' command to all of the other remote units. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." (7:4-13). FIG. I, II, V, VIII; IX said master network timing means – *see row 9 above*
20. priority bit	11	A bit used to convey the relative importance of the communication. Intrinsic Support: FIGS. 1, 3, element 14; FIG. 5, 8; "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect	a bit defining a remote unit's relative importance as compared to subsequent units, set by the user at initialization of the master unit Intrinsic Support: "In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as

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		to transmission time; and priority assigned reservation request for long poll responses." 1:63-2:1; "In order to accommodate longer message lengths from a remote unit to the master unit, a remote unit can append a request for additional time onto its message to the master unit. The master unit will then compare the priority of the requesting remote unit to the priority of subsequent units and make a decision as to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." 2:18-26; "As is disclosed in FIG. VI, the first step in the initialization of the master unit is to input the directory of users. This is an address entry for each host application drop. The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate	to whether to allow the requesting remote unit to use the time division multiple access slots of subsequent units." (2:18-26). "Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each "drop" or remote unit, priority assignments, drop addressing, and port speed assignments." (2:68-3:6). "As is disclosed in FIG. VI, the first step in the initialization of the master unit is to input the directory of users. This is an address entry for each host application drop. The next step is to input the address priority level. This is followed by an initialization of such system parameters as frame period, number of time slots per subframe, inbound message lengths, inbound and outbound transmission rates (notice that aggregate burst rate must be higher than the sum of the independent port rates so as to accommodate individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments." (5:10-22).

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		individual ports along with associated overhead), priority assignments, drop addressing and, port speed assignments. This information is stored in the network timing and control processor." 5:10-23, "Finally, "set-up" parameters are transmitted from the master unit to the remote units so as to establish remote unit transmit clock advances, priority level, and inbound time slot assignments for the primary and diagnostic channels. The remote unit verifies receipt to the master unit." 5: 40-45; "The master unit sends a message to one of the remote units. An inbound message is received from one of the remote units. The address, cyclic redundancy calculation (i.e. checksum) and priority level are checked. If any of these values are invalid, the master unit retransmits to the remote unit. If these values are valid and there is no reservation request, the message is output to the appropriate application host port at the master end. This process is continually repeated for each application in each remote unit. If the aforementioned values are valid but there is a reservation request, then the message is queued in	"Finally, "set-up" parameters are transmitted from the master unit to the remote units so as to establish remote unit transmit clock advances, priority level, and inbound time slot assignments for the primary and diagnostic channels." (5:39-44). "The remote unit receives set-up parameters such as clock advance, priority level and inbound time slot assignment for the primary and diagnostic framing and set-up information to the master unit." (5:5:53-56). "The master unit sends a message to one of the remote units. An inbound message is received from one of the remote units. … If the aforementioned values are valid but there is a reservation request, then the message is queued in the event that there is a higher priority request or acknowledged and completely received in the event that there is no higher priority request." (5:58-6:5). "For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays." (6:68-7:3).

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		the event that there is a higher priority request or acknowledged and completely received in the event that there is no higher priority request. After the complete message is received, its address, checksum and priority are validated. If these values are valid, the message is output to the host port. If the values are not valid, the initial step of an outbound transmission from the master to the remote is returned. FIG. IX discloses the normal operation of a drop or remote unit. The remote unit receives and buffers a DTE poll response message. The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." 5:59-6:24;	"The master unit clocks the received message bits to expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an 'authorization to transmit' command and transmits a 'transmit inhibit' command to all of the other remote units. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." (7:4-13). "The Applicant has amended Claim 14 in accordance with the Examiner's observation that 'bits' should read 'bit'." (File History, March 5, 1990 Amendment, p.6). FIG. I, II, V, VIII; IX

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		"The subframe time slot is sized for the dominant poll response message length for the application. For longer transmissions, the remote unit sets the reservation bits to identify the required number of additional time slots. The priority bit or bits define the remote's relative importance in reducing poll-response delays. The master unit clocks the received message bits to the expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an "authorization to transmit" command and transmits a "transmit inhibit" command to all of the other remote units. Each of these outbound transmissions are error protected so that remote transmission contention is extremely unlikely. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." 6:66-7:14	
21.	said time slot comprises a format so as to include a	11	Rembrandt does not believe this term requires construction. In the alternative: the time slot is formatted to include a preamble, a poll response data bit, reservation bits, at least one priority bit	the single time slot to which each application is assigned is formatted to include a preamble, a poll response data bit, said reservation request bits, at least one priority bit and error detection bit

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preamble, a poll response data bit, said reservation bits, at least one priority bit and error detection bit		[defined above] and error detection bit. Intrinsic Support: "The remote unit computes the reservation request and the CRC (cyclic redundancy check or checksum) bits. The CRC bits provide error detection for both overhead and transmit port primary data bits. The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." 6:13-24; "All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." 6:57-60.	Intrinsic Support: "All inbound transmissions contain a preamble, poll response data bits, reservation request bits, at least one priority bit and error detection bits." (6:57-60). "Reservation request processor 14 allows a drop or remote unit to request more than a single time slot for longer messages. Reservation request processor 14 communicates such a granted request to the network timing and control processor 12." (3:7-11). "The subframe is further subdivided into slots, one for each application." (4:56-57). "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits." (4:62-67). "The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and

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			synchronize so as to reduce guard time) transmit clock. This block of data includes preamble data, reservation request, priority level, delimiter and CRC bits." (6:17-24). "The master unit clocks the received message bits to expansion buffer 30 and checks the reservation and priority bits for error. If no errors are detected, the master responds to the remote with an 'authorization to transmit' command and transmits a 'transmit inhibit' command to all of the other remote units. The authorized remote commences transmission on the next available time slot and continues until the message transmission has been completed. During this period the expansion buffer clocks data bits to the host." (7:4-13). FIG. I, II, V, VIII; IX
22. transmitting from said master unit to each of said respective remote units the	14(d)	Rembrandt does not believe this term requires construction. In the alternative: the master unit [defined above] sends each remote unit [defined above], the transmission time between the master unit [defined above] and each respective remote unit, and each remote unit uses its transmission time (from the master unit [defined above] to that	during initialization of the master unit before the remote units transmit data, the master unit transmits to each remote unit the transmission time between the master unit and remote unit for each combination of remote unit and application Intrinsic Support:

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transmission time between said master unit and said respective remote unit, each of said respective remote units usin*g* said transmission time to adjust initiation of said slots		remote unit) to adjust when that remote unit initiates transmission. Intrinsic Support: Abstract; FIGS 1 & 3, elements 12, 20, 32; FIGS. 1-4, 6-9; "Additionally, the ranging calculations, that is, the master unit calculation of the time a signal takes to go from the master unit to any remote unit and vice versa, is stored in the timing and control block 46 where it is used for time advancing the transmit clock." 3:65-4:2; "The basic features of this method and apparatus are time division multiplexed outbound transmissions from the master to the remote units for data and control; time division multiple access transmissions inbound from the remote units to the master unit; master to remote ranging with respect to transmission time; and priority assigned reservation request for long poll responses. A channel rate exceeding the aggregate port rate is required in order to transmit effectively all of the information from the remote units and allow for	FIGS I-III; VI-VII. "The initialization phase of operation also includes a ranging calculation for each combination of remote unit (or "drop") and application. The master unit sends a message which makes a round-trip between the master unit and the individual remote unit. The delay period is stored in a library table in the network timing and control processor 12 so that the remote to master unit communication is synchronized, thereby reducing guard time required between successive transmissions and increasing the efficiency of the system." (5:24-34). "Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12. Network timing and control processor 12 uses firmware or software to implement clock drift reset functions, guard time predict functions, burst receiver control functions, reservation assignment functions, cyclic redundancy check (crc) "checksum" calculations, arq functions, remote transmit control functions and user library update functions such as activity rate and frame parameters.

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		control format messages. All remote units (or "drops") receive messages outbound from the control unit and respond in a unique time period assigned to each host application. Contention between applications is thereby avoided due to the fact that each application is assigned such a unique time period. By ranging or measuring the round-trip transmission or delay time between the master unit and each remote unit, and storing these times in a table so as to accurately synchronize the transmissions in a time division multiple access mode, the "guard time" separating inbound transmissions from interfering with each other can be minimized thereby increasing system efficiency." 1:63-2:17; "The master unit 10 also provides, in addition to primary traffic flow over the channel outbound to remote units, a diagnostic channel which can be inband, and any control information necessary to update clock drifts, perform new ranging, etc." 3:25-29; "The ranging receiver 32 receives data from the demodulator 28 during an initial training period (to be described later) so as to store round trip	Additionally, network timing and control processor 12 stores user-input initialization parameters including network clock framing periods, slot and subframe assignments, inbound and outbound burst length for each 'drop' or remote unit, priority assignments, drop addressing, and port speed assignments." (2:57-3:6). "The aggregate rate multiplexing module 16, in response to commands from the network timing and control processor 12, sets up the timing and bit interleaving of the various application inputs from the various input ports of the primary channel multiplexer 18 and of the overhead and control bits required for outbound control of the remote units from the ranging and network initialization generator 20. The output of the aggregate rate multiplexer 16 is input to the time division multiplexed modulator 22 which transmits the data to the various drops or remote units (see FIG. II). The time division multiplexed modulator 22 is typically a baseband modulator for digital applications." (3:12-24). "Demodulator 28 provides digital data to the expansion buffers 30, the ranging receiver 32, the reservation request processor 14 and the bit/baud

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		transmission times to each remote unit. This allows an optimization in synchronization of the time division multiple access process, thereby reducing "guard time" between the reception of data from the various remote units thereby increasing the total data transfer rate of the system." 3:42-49; "Additionally, the ranging calculations, that is, the master unit calculation of the time a signal takes to go from the master unit to any remote unit and vice versa, is stored in the timing and control block 46 where it is used for time advancing the transmit clock." 3:65-4:2; "FIG. V discloses a typical subframe. A subframe is divided into N time slots, each separated by a guard time. Each slot contains a preamble, message bits, reservation request bits, priority bits, and error detection bits. The reservation and priority bits may be replaced by address bits. For example, five bits would permit up to 32 drops. The address bits would be an identifier to the master. The master could then monitor remote clock accuracy, monitor drop transmission events, perform ranging, etc." 4:62-5:3;	timing processor 34." (3:35-38). "The ranging receiver 32 receives data from the demodulator 28 during an initial training period (to be described later) so as to store round trip transmission times to each remote unit. This allows an optimization in synchronization of the time division multiple access process, thereby reducing "guard time" between the reception of data from the various remote units thereby increasing the total data transfer rate of the system." (3:42-49). FIG. II "Additionally, the ranging calculations, that is, the master unit calculation of the time a signal takes to go from the master unit to any remote unit and vice versa, is stored in the timing and control block 46 where it is used for time advancing the transmit clock." (3:65-4:2). "Initialization of the remote drops is disclosed in FIG. VII. The user inputs . . . The remote unit returns of 'loops-back' the ranging signal from the master unit. 5:45-52

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		"The initialization phase of operation also includes a ranging calculation for each combination of remote unit (or "drop") and application. The master unit sends a message which makes a round-trip between the master unit and the individual remote unit. The delay period is stored in a library table in the network timing and control processor 12 so that the remote to master unit communication is synchronized, thereby reducing guard time required between successive transmissions and increasing the efficiency of the system." 5:24-34; "2. The master unit periodically transmits a network clock reading to all remotes and performs a roundtrip delay transmission calculation ("ranging") to each remote unit. The master unit informs each remote unit of its precise round trip value." 6:32-36; "This invention relates to an apparatus and method for a master unit in a multidrop network to communicate to and from a plurality of remote units, using a plurality of host applications using half duplex polled protocols, through the use of time division multiple access techniques." 1:5-10;	"The remote unit transmits the first block of data, and possibly a reservation request on the inbound channel at a predetermined time in accordance with the "time advanced" (to allow for transmission time and synchronize so as to reduce guard time) transmit clock." 6:17-22.

U.S. Patent No. 4,937,819	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"Referring now to the drawings in detail wherein like numerals refer to like elements throughout the several views, master unit 10 for digital applications is shown FIG. I. Master unit 10 includes a network timing and control processor 12." 2:56-61; "10. The master unit can recognize whether a remote clock is drifting and so inform the remote with a fast or slow correction value. Such information can be extracted from the actual time of arrival compared with the expected time of arrival at the master unit and the preamble which identifies the transmitted remote." 7:15-20.	

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U.S. Patent No. 5,719,858 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
1. data communications apparatus/ communications apparatus/data communications equipment	1(a), 7(a), 8, 9(a), 10, 11(a), 15(a), 20(a), 26	Rembrandt does not believe this term requires construction. In the alternative: a data communication device. Intrinsic Support: Abstract; FIG. 3, element 200; "Communications equipment horn as a 'network access unit' (NAU) typically provides frame-relay-type services between a local communications network and a network facility, like a T1 facility. The NAU messages the flow of data between the local communications network and the network facility in both directions. To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design	network access unit (a single device that manages the flow of data between a local network and a network facility) Intrinsic Support: FIGS. 1-4, 8A-C "Communications equipment horn as a "network access unit" (NAU) typically provides frame-relay-type services between a local communications network and a network facility, like a T1 facility. The NAU messages the flow of data between the local communications network and the network facility in both directions." (1:12-17). "For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services." (1:19-20). "NAM 105 provides the interface between time-division-multiplexing (TDM) bus 104 and network

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		tradeoffs in both the complexity and cost of an NAU." 1:12-26; In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:49-65; "An illustrative block diagram of an NAU	facility 106, which is representative of a T1 facility." (1:33) "One prior art approach of designing an NAU to support both synchronous data and packet data is shown in FIG. 1. . . ." (1:28-54). "Another prior art approach is illustrated in FIG 2, which is similar to FIG. 1. . . ." (2:15-27). "I have realized an alternative approach to the design of <u>TDM-based equipment</u> that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling." (2:42-45) (emphasis added). "Each packet application module <u>includes its own TDM bus interface</u> and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint." (2:57-61). "FIG. 3 shows an illustrative block diagram of a time-division-multiplexing-only <u>network access unit</u> in accordance with the principles of the invention;" (3:20-22).

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		embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility." 3:39-48;	"An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." (3:39-53). "Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an 'application specific integrated circuit' (ASIC)." (3:62-4:1). "Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to

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			packet/TDM interface 310 via line 307, buffer 315, and line 309." (4:15) "In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, <u>each module, or circuit board, can have an address associated either via</u> a 'software-controlled' configuration . . . or by a hardware setting that specifically associates a particular address with <u>a particular position in the system, e.g., what slot the circuit board is plugged into.</u>" (7:45-53). "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." (8:8-23; *see also* 8:24-9:17). "The only hardware function required to support such strategies is the combination of the PREQ signal and

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			PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." (10:31-42). "As noted above, the above description assumed that the packet/TDM interface was incorporate in a single ASIC bus interface chip . . . an ASIC having a much larger gate-count may be needed." (10:44-58). Examiner's Statement of Reasons for Allowance, 10/1/97 *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance.
<u>2.</u> bus	1(b), 7(b), 8,	Rembrandt does not believe this term requires construction. In the alternative: one or more	hardware line(s) within a device used for data transfer among its components

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	9(b), 10, 11(b), 15(a), 20(a), 26	conductors that are used as a path for transmitting information from any of several sources to any of several destinations. Intrinsic Support: FIGS. 3, 4 - element 204, 5, 7; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a 'multiple-access packet channel.' This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet	Intrinsic Support: FIGS. 1-4, 8A-C "Communications equipment horn as a "network access unit" (NAU) typically provides frame-relay-type services between a local communications network and a network facility, like a T1 facility. The NAU messages the flow of data between the local communications network and the network facility in both directions." (1:12-17). "For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services." (1:19-20). "NAM 105 provides the interface between time-division-multiplexing (TDM) bus 104 and network facility 106, which is representative of a T1 facility." (1:33) "One prior art approach of designing an NAU to support both synchronous data and packet data is shown in FIG. 1. . . ."(1:28-54).

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		application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in **FIG. 3.** NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the	"Another prior art approach is illustrated in FIG 2, which is similar to FIG. 1. . . ." (2:15-27). "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling." (2:42-45) (emphasis added). "Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint." (2:57-61). "FIG. 3 shows an illustrative block diagram of a time-division-multiplexing-only network access unit in accordance with the principles of the invention;" (3:20-22). "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200

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		art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules**."** 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the	includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." (3:39-53). "Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an 'application specific integrated circuit' (ASIC)." (3:62-4:1) "Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309." (4:15) "In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For

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		"outbound" TDM is similarly used for status and control information**."** 4:25-36; "In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC	example, <u>each module, or circuit board, can have an address associated either via</u> a 'software-controlled' configuration . . . or by a hardware setting that specifically associates a particular address with <u>a particular position in the system, e.g., what slot the circuit board is plugged into.</u>" (7:45-53). "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." (8:8-23; *see also* 8:24-9:17). "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a

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		is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:43-6:5; "Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be	corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." (10:31-42). "As noted above, the above description assumed that the packet/TDM interface was incorporate in a single ASIC bus interface chip . . . an ASIC having a much larger gate-count may be needed." (10:44-58). "The prior art does not teach a data communications apparatus and method including a TDM bus, with a portion of the bandwidth allocated to packet data; …" (Office Action, 4/4/97, at p. 5) Examiner's Statement of Reasons for Allowance, 10/1/97 *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17	
_3._ time-division multiplexed bus	1, 7, 8, 9, 10, 11, 15, 20, 26	A bus having a bandwidth partitioned into a defined, repeated sequence of time slots, that is shared by two or more sources of data by limiting each source's transmission opportunities to discrete intervals of time. Intrinsic Support: FIGS. 3 & 4, element 204; FIGS. 5 & 7; Abstract; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g.,	a bus having its bandwidth partitioned into a repeating sequence of time slots defined to be used in the same way during each repetition, whereby only one data source can successfully transmit over the bus at any one discrete interval of time Intrinsic Support: "FIG. 3 shows an illustrative block diagram of a time-division-multiplexing-only network access unit in accordance with the principles of the invention;" 3:20-22. "FIG. 5 shows a representation of a sequence of time division multiplexing frames in accordance with the principles of the invention." "Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:21-23.

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		synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205,	"In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:54-57 "In a feature of the invention, a contention scheme for accessing the "multiple-access packet channel" is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3. "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206." 4:25-31. "In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application

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		synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules." 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is	modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 5:2-10. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the

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		shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the 'outbound' TDM is similarly used for status and control information." 4:25-36; "(Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 5:5-10; "In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous	"multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14. "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner." 6:53-61. "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel"

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		sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a '"bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of	for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 6:65-7:8.

"FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module." 7:25-30.

"The value of the count is the ID number for the "bit time-slot." All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times." 7:38-41.

"It is assumed that each packet application module counts "bit time-slots" of the "multiple-access packet channel" beginning with "bit time-slot" 1 of frame 1, |

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		packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:43-6:5; "Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "The remainder of this description will focus on outbound packet traffic." 6:52-64; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17.	which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the "bit time-slot" to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in "bit time-slot" 1 of time-slot 1 of frame 1, "bit time-slot" 8 of time-slot 1 of frame 1, "bit time-slot" 7 of time-slot 2 of frame 1 etc." 7:63-8:7. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. FIGS 3-8C

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4. packet data	1(b), 7(d), 8, 9(d), 10, 11(d), 15(a), 20(a), 26	Variable bit rate data. Intrinsic Support: Abstract; "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the	data that travels in packets Intrinsic Support: FIGS. 1-8C "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11. "Communications equipment horn as a 'network access unit' (NAU) typically provides frame-relay-type services between a local communications network and a network facility, like a T1 facility. The NAU messages the flow of data between the local communications network and the network facility in both directions. To provide the most

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		asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56	flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services." 1:12-23. "However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:24-27. "In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:61-65. "In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g.,

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			virtual address, if it is not their packet, it is just dropped." 6:41-51. "Additionally, the prior art of record does not teach that each packet application module includes its own TDM bus interface, accepts the entire received packet stream from the network access module, and either filters the packets using the address field or forwards the packet data to a packet service." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p.1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance
5. portion	1(b), 7(b), 8, 9(c), 10, 11(c), 15(c), 20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: a part of a whole. Intrinsic Support: "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a	fixed amount less than the whole Intrinsic Support: FIGS 5, 8A "Unfortunately, the instantaneous, or peak, data rate of all outbound packet streams taken together may be greater than the "fixed amount of TDM bandwidth" allocated for packet data on the network interface.

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		network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention,	These peak data rates create a large demand on both the overall packet bus capacity and on the packet handling requirements of packet manager 110. For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic.." 1:65-2:10. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the

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		the time-slots allocated by NAM 205 to the packet application modules are the 'multiple-access packet channel.' In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth	TDM bandwidth to each packet application module." 4:56-62. "In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." 5:17-20 "Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load." 6:18-22. "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "The prior art does not teach a data communications apparatus and method including a TDM bus, with a portion of the bandwidth allocated to packet data; …" (Office Action, 4/4/97, at p. 5) "The packet data sources are coupled to a single time division multiplexing (TDM) bus for communicating

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		is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17	data to a network access module, wherein a portion of the TDM bandwidth allocated to packet data is treated as a multiple access packet channel." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p. 1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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6. portion of the bandwidth is allotted to packet data	1(b)	Rembrandt does not believe this term requires construction. In the alternative: one or more time slots allotted to sources of packet data. Intrinsic Support: "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots

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		application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information.	yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment

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		The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." 6:15-24;	information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See row 5 above*

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		"Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17 "The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the 'multiple-access packet channel' is closely matched (or equal) to that allocated for packet traffic across network facility 206." 4:62-5:2; "In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the	

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		assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted)." 9:22-30.	
7. second portion of the predefined bandwidth	7(d), 9(d), 11(d)	Rembrandt does not believe this term requires construction. In the alternative: for transmitting packet data in a second portion of the predefined bandwidth [defined above]. Intrinsic Support: Abstract; FIGS. 6 & 8, "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame

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		bandwidth allocated to packet data." 2:49-57; "In a feature of the invention, a contention scheme for accessing the "multiple-access packet channel" is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case,	is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is

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		each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules." 4:56-5:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header,	initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. <u>During this initialization,</u> NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel."￼ Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See row 5 above*

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		e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the	

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		"access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." During this "access period," a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the "access window" is frozen at the current packet application module and does not advance until that packet application module releases the "multiple-access packet channel." Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the "multiple-access packet channel." In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several "bit time-slots," or clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization.	

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		FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module. In a system with N packet application modules, each "bit time-slot" of the "multiple-access packet channel" is counted in a repeating sequence from 0 to N-1 starting at some arbitrary "bit time-slot" by each packet application module. In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." The value of the count is the ID number for the "bit time-slot." All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a priori, the time-slots associated with the "multiple-access packet channel." In combination with this, each packet application module is configured with an unique ID number, which can	

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		be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of "bit time-slots" may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts "bit time-slots" of the "multiple-access packet channel" beginning with "bit time-slot" 1 of frame 1, which is associated with the count value of 0. Each packet	

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		application module waits for its ID number to equal the count, or ID number, of the "bit time-slot" to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in "bit time-slot" 1 of time-slot 1 of frame 1, "bit time-slot" 8 of time-slot 1 of frame 1, "bit time-slot" 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are "packet request" (PREQ) and "packet hold" (PHOLD). It is assumed these signals are bussed among the packet application modules as simply "open collector" as known in the art which allows them to be logically "OR"ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those "bit time-slots" assigned to the "multiple-access packet channel." The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the "bit time-slot" of the "multiple-access packet channel," i.e., the value of the count. The next two rows represent the state of the PREQ	

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		and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the "bit time-slot" ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the "bit time-slot" and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the "bit time-slot" and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next "bit time-slot,"	

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		t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC	

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		inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be	

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		implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the "multiple-access packet channel." The counter included within packet/TDM interface 310 rims continuously and is controlled	

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		by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the "access	

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		window" in step 525. Once the "access window" matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the "bit time-slot" ID number, TDM/packet interface 310 asserts the PREQ signal in step 530. In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the "multiple-access packet channel" continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the "multiple-access packet channel." Within this general method, different approaches	

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		may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period.	

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		The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus.´6:41-10:42	
8. the allocated portion of the bandwidth	15(d)	Rembrandt does not believe this term requires construction. In the alternative: the allocated portion of the bandwidth [defined above]. Intrinsic Support: Abstract; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g.,	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated

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		synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to	portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38.

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		control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access	"A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See row 5 above*

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		packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources. ´6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as	

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		opposed to the "bit-time slots," described above." 11:12-17	
9. allocating a portion of the bandwidth of the time-division multiplexed bus to the plurality of packet data sources	15(c)	Rembrandt does not believe this term requires construction. In the alternative: allocating a portion of the bandwidth [defined above] of the time-division multiplexed bus [defined above] to the plurality of packet data [defined above] sources. Intrinsic Support: Abstract; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated

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		bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these	to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots

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		DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness.	associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See row 5 above*

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		Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17; "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11;	

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		"To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56	
10. allocating a portion of the bandwidth of the time-division multiplexed bus	20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: the allocated portion of the bandwidth [defined above].	portion of the TDM data transfer capacity, fixed at initialization, in which all packet data from the plurality of packet data sources that share it must travel, and in which only such packet data may travel Intrinsic Support: FIGS. 5-8C

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			"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only

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			counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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11. portion of the bandwidth	1, 15, 20	One or more time slots of the bandwidth. Intrinsic Support: FIGS. 5-7; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet	*portion - see row 5 above* See row 6 above for the use of "portion of the bandwidth" in the context of the actual and complete claim language Intrinsic Support: FIGS. 5-8C "Unfortunately, the instantaneous, or peak, data rate of all outbound packet streams taken together may be greater than the "fixed amount of TDM bandwidth" allocated for packet data on the network interface. These peak data rates create a large demand on both the overall packet bus capacity and on the packet handling requirements of packet manager 110. For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic.." 1:65-2:10.

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		application module" 4:56-62; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth	"In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load." 6:18-22. "The prior art does not teach a data communications apparatus and method including a TDM bus, with a portion of the bandwidth allocated to packet data; …"

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		allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:57-5:10; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the 'multiple-access packet channel.' In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated	(Office Action, 4/4/97, at p. 5) "The packet data sources are coupled to a single time division multiplexing (TDM) bus for communicating data to a network access module, wherein a portion of the TDM bandwidth allocated to packet data is treated as a multiple access packet channel." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p. 1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple

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		to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of	packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added).

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		every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the	

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		"multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted.	

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		As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules. The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources. Any method used for implementing a "multiple-access packet channel" should be designed to achieve as close to 100% bandwidth efficiency as	

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		possible with no negative throughput effects due to congestion. The method should also have no inherent priority bias among the packet sources so that priorities may be enforced selectively if needed, preferably in software on the packet application modules. These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe. Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction. In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its	

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		header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 5:20-6:64; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth.	

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		Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the	

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		time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period." 10:11-31; "In addition, although illustrated in the context of a T1 network facility, the inventive concept applies to other network facilities as well, e.g., fractional T1, digital data service (DDS), T3, etc. Further, more than one "multiple-access packet channel," can exist. For example, a first plurality of packet application modules may be assigned to a first group of time-slots, e.g., time-slots 1-6, for transmitting packet data, while a second plurality of packet application modules is assigned to a second group of time-slots, e.g., time-slots 7-12, for transmitting packet data. Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above. "Also, because the bandwidth of a TDM bus may	

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		be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:3-17.	
12. portion of the predefined bandwidth	7, 9, 11	One or more time slots of the predefined bandwidth. Intrinsic Support: FIGS. 5-7; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57;	*portion - see row 5 above* See row 6 above, for the use of "portion of the bandwidth" in the context of the actual and complete claim language Intrinsic Support: FIGS. 5-8C "Unfortunately, the instantaneous, or peak, data rate of all outbound packet streams taken together may be greater than the "fixed amount of TDM bandwidth" allocated for packet data on the network interface. These peak data rates create a large demand on both the overall packet bus capacity and on the packet handling requirements of packet manager 110. For example, once the packet application modules exceed

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		"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module" 4:56-62; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely	their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic.." 1:65-2:10. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "Bandwidth efficiency is a measure of how closely

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		matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:57-5:10; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the 'multiple-access packet channel.' In this example, it is assumed that every time-frame	the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load." 6:18-22. "The prior art does not teach a data communications apparatus and method including a TDM bus, with a portion of the bandwidth allocated to packet data; …" (Office Action, 4/4/97, at p. 5) "The packet data sources are coupled to a single time division multiplexing (TDM) bus for communicating data to a network access module, wherein a portion of the TDM bandwidth allocated to packet data is treated as a multiple access packet channel." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p. 1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels . . . The remaining time-slots are allocated

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		is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42;	to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots

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		"In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is	associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added).

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		assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1	

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		through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted. As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules. The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also	

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		measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources. Any method used for implementing a "multiple-access packet channel" should be designed to achieve as close to 100% bandwidth efficiency as possible with no negative throughput effects due to congestion. The method should also have no inherent priority bias among the packet sources so that priorities may be enforced selectively if needed, preferably in software on the packet application modules. These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe. Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound	

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		direction. In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 5:20-6:64;	

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		"The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic	

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		across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period." 10:11-31; "In addition, although illustrated in the context of a T1 network facility, the inventive concept applies to other network facilities as well, e.g., fractional T1, digital data service (DDS), T3, etc. Further, more than one "multiple-access packet channel," can exist. For example, a first plurality of packet application modules may be assigned to a first group of time-slots, e.g., time-slots 1-6, for transmitting packet data, while a second plurality of packet application modules is assigned to a second group of time-slots, e.g., time-slots 7-12, for transmitting packet data. Also, because the	

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		bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above. "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:3-17.	
13. having a predefined bandwidth	7(b), 8, 9(b), 10, 11(b)	Rembrandt does not believe this term requires construction. In the alternative: having a predefined bandwidth [defined above]. Intrinsic Support: Abstract; FIGS. 6 & 8. "In an embodiment of the invention, a plurality of	first and second portions of the TDM bandwidth fixed during initialization Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the

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		packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus	packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 (emphasis added). "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have

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		(not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i	been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this _initialization_, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). _See also row 5 above_ _See also_ '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be	

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		combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17.	
14. predefined bandwidth	7, 9, 11	A predefined amount of data that can be carried in a unit of time. Intrinsic Support: FIGS. 5-7; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated	first and second portions of the TDM bandwidth fixed during initialization Intrinsic Support: FIGS. 5-8C "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62. "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0

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		portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module" 4:56-62; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet	channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz." 5:21-32 (emphasis added). "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing

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		channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:57-5:10; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the 'multiple-access packet channel.' In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is	signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:17-31 (emphasis added). *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See also row 5 above*

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		also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these	

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		DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple	

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		TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and	

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		ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted. As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules. The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through	

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		the system under bandwidth contention with multiple packet sources. Any method used for implementing a "multiple-access packet channel" should be designed to achieve as close to 100% bandwidth efficiency as possible with no negative throughput effects due to congestion. The method should also have no inherent priority bias among the packet sources so that priorities may be enforced selectively if needed, preferably in software on the packet application modules. These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe. Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction. In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application	

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		modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 5:20-6:64; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness.	

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		Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port.	

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		For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period." 10:11-31; "In addition, although illustrated in the context of a T1 network facility, the inventive concept applies to other network facilities as well, e.g., fractional T1, digital data service (DDS), T3, etc. Further, more than one "multiple-access packet channel," can exist. For example, a first plurality of packet application modules may be assigned to a first group of time-slots, e.g., time-slots 1-6, for transmitting packet data, while a second plurality of packet application modules is assigned to a second group of time-slots, e.g., time-slots 7-12, for transmitting packet data. Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system.	

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		Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above. "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:3-17.	
15. [for communicating synchronous data in a] first portion of the predefined bandwidth	7(c), 8, 9(c), 10, 11(c)	Rembrandt does not believe this term requires construction. In the alternative: for transmitting synchronous data in a first part of the predefined bandwidth [defined above]. Intrinsic Support: Abstract; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to	portion of the TDM data transfer capacity, fixed at initialization, in which all synchronous data from the plurality of synchronous data sources must travel, and in which only such synchronous data may travel Intrinsic Support: FIG. 5 (OTHER TDM CHANNELS); 8A "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0

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		the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art.	channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. <u>The remaining time-slots are allocated to synchronous data and control/status information</u>." 5:15-30 (emphasis added). "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57. *See also rows 5 & 6 above* *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.)	

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		Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above."	

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		11:12-17	
16. synchronous data	7, 8, 9, 11	Constant bit rate data. Intrinsic Support: FIG. 3, element 220-1 – 220-n; FIG. 4, element 204; FIGS. 5 & 7; Abstract; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM	data sent synchronously through TDM without packetization Intrinsic Support: "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." (1:6-11) "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services." (1:18-23) "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition,

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		bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment,	provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." (2:42-48) FIGS. 1-8C *See also* 1:1-2:40; 2:49-3:12; 4:56-5:10 *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See also rows 4 & 6*

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		to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules." 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on	

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		the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and control information." 4:25-36; "In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access	

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		packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted. " 5:43-6:5; "Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "In accordance with the invention, a Time-division	

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		Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:52-64; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17.	
17. plurality of packet data	1(c), 7(d), 8, 9(d),	Rembrandt does not believe this term requires construction. In the alternative: more than one	circuit boards inside the apparatus that each has its own interface connected to the TDM bus that sends

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sources coupled to the time division multiplexed bus	10, 11(d)	source of packet data that are operatively connected to the time-division-multiplexed bus. Intrinsic Support: FIGS. 3 & 4 – elements (215 l-n); "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a 'multiple-access packet channel.'" 2:49-54; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56	only packet data Intrinsic Support: FIGS. 3-4 "Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed packet stream for transmission to an opposite endpoint." (2:56-61.) "Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an 'application specific integrated circuit' (ASIC)." 3:62-4:1 "Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309." 4:15 "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module." 2:49-53.

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			"In combination with this, <u>each packet application module</u> is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or <u>circuit board</u>, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., <u>what slot the circuit board is plugged into.</u>" 7:45-53 (emphasis added). "The NAU messages the flow of data between the local communications network and the network facility in both directions. To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU.

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			One prior art approach of designing an NAU to support both synchronous data and packet data is shown in FIG. 1. NAU 100 includes network access module 115-1 105, synchronous application modules 120-1 to 120-n, packet application modules 115-1 to 115-n, and packet manager 110. NAM 105 provides the interface between time-division-multiplexing (TDM) bus 104 and network facility 106, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:16-40. "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:35-40. "NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application

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			modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place." 3:46-59.

"An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules |

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			couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." 3:39-53.

"Packet interface processor 305 communicates packet data between packet/TDM interface 310 and line 304. The latter is representative of any one of a number of facilities for coupling packet application module 215-n to a packet system. For example, line 304 could be a local area network, or a dedicated facility to a "router" or a packet data terminal. Packet interface processor 305 performs packet handling, e.g., it provides the physical and link layer connections for packet transmission as known in the art, e.g., it checks for addresses, errors, etc., on the packets." 4:4-14

"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. |

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			This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "The remaining time-slots are allocated to synchronous data and control/status information." 5:28-30. "Additionally, the prior art of record does not teach that each packet application module includes its own TDM bus interface, accepts the entire received packet stream from the network access module, and either filters the packets using the address field or forwards the packet data to a packet service." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p.1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance
18. coupling a plurality of packet data	15(b), 20(c), 26	Rembrandt does not believe this term requires construction. In the alternative: operatively connecting each of a number of sources of packet	circuit boards inside the apparatus that each has its own interface connected to the TDM bus that sends

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sources to the time division multiplexed bus		data to the time-division multiplexed bus [defined above]. Intrinsic Support: Abstract; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed	only packet data Intrinsic Support: FIGS. 3-4 "Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed packet stream for transmission to an opposite endpoint." (2:56-61.) "Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an 'application specific integrated circuit' (ASIC)." 3:62-4:1 "Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309." 4:15 "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module." 2:49-53.

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		fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated	"In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into." 7:45-53 (emphasis added). "The NAU messages the flow of data between the local communications network and the network facility in both directions. To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU.

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		to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme	One prior art approach of designing an NAU to support both synchronous data and packet data is shown in FIG. 1. NAU 100 includes network access module 115-1 105, synchronous application modules 120-1 to 120-n, packet application modules 115-1 to 115-n, and packet manager 110. NAM 105 provides the interface between time-division-multiplexing (TDM) bus 104 and network facility 106, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:16-40. "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:35-40. "NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application

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		affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17; "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of	modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place." 3:46-59. "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules

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		packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56	couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." 3:39-53. "Packet interface processor 305 communicates packet data between packet/TDM interface 310 and line 304. The latter is representative of any one of a number of facilities for coupling packet application module 215-n to a packet system. For example, line 304 could be a local area network, or a dedicated facility to a "router" or a packet data terminal. Packet interface processor 305 performs packet handling, e.g., it provides the physical and link layer connections for packet transmission as known in the art, e.g., it checks for addresses, errors, etc., on the packets." 4:4-14 "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules.

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			This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "The remaining time-slots are allocated to synchronous data and control/status information." 5:28-30. "Additionally, <u>the prior art of record does not teach that each packet application module includes its own TDM bus interface</u>, accepts the entire received packet stream from the network access module, and either filters the packets using the address field or forwards the packet data to a packet service." (Examiner's Statement of Reasons for Allowance, 10/1/97, at p.1) *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance
<u>19.</u> A plurality of synchronous data sources	7(c), 8, 9(c), 10,	Rembrandt does not believe this term requires construction. In the alternative: more than one source of synchronous data that are operatively	circuit boards inside the apparatus that each has its own interface connected to the TDM bus that sends only synchronous data

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coupled to the time-division multiplexed bus	11(c)	connected to the time-division-multiplexed bus [defined above]. Intrinsic Support: FIG. 3, element 220-1 – 220-n; FIG. 4, element 204; FIGS. 5 & 7; Abstract; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM	Intrinsic Support: (showing how each Packet Application Module and Synchronous Application Module has its own interface) FIGS. 3-4 "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:35-40. "Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed packet stream for transmission to an opposite endpoint." (2:56-61.) "Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309." 4:15 "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM

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		bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment,	bus for communicating data to a network access module." 2:49-53. "In combination with this, <u>each packet application module</u> is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or <u>circuit board</u>, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., <u>what slot the circuit board is plugged into.</u>" 7:45-53 (emphasis added). "NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM

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		to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules." 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on	bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place." 3:46-59. "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." 3:39-53. See also '858 patent file history at 4/4/97 Office

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		the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and control information." 4:25-36; "In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access	Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:43-6:5; "Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "In accordance with the invention, a Time-division	

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		Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:52-64; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17	
20.	plurality of packet data sources…that	1(c)	Rembrandt does not believe this term requires construction. In the alternative: more than one source of packet data that each use time slots that	without the need for a central packet manager, each packet data source treats the allotted bandwidth as a single channel by contending for use of the entire

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share the allotted bandwidth for transmitting packet data		are allotted to packet data. Intrinsic Support: "FIGS. 3 & 4 – elements (215 l-n), FIGS. 6 & 8; ""In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In a feature of the invention, a contention scheme for accessing the 'multiple-access packet channel' is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3; "In accordance with the invention, a portion of the	channel in which no time slot is assigned to any particular packet data source Intrinsic Support: "I have realized an alternative approach to the design of TDM-based equipment . . . In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:40-48. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM

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		bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the 'multiple-access packet channel' with the other packet application modules." 4:56-5:5; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is	channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated

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		also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a 'multiple-access packet channel' with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the 'multiple-access packet channel' for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The 'multiple-access packet channel'	portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10.

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		in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the 'multiple-access packet channel.' An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a 'bit time-slot.' It should be noted that the term 'time-slot' refers to a collection of 'bit time-slots.' Time-slots 1-6 represent the 'multiple-access packet channel.' As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of 'bit time-slots' within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with 'bit time-slot' 7 in time-slot 4, of frame 1, and ends with 'bit time-slot 3' in time-slot 2 of frame 4.	"As such, the starting point of a packet may lie anywhere in the 'multiple access packet channel.'" 5:47-52. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "Any method used for implementing a 'multiple - access packet channel' should be designed to achieve as close to 100% bandwidth efficient as possible. . . ." 6:26-32 "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet

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		As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:20-6:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the 'multiple-access packet channel' for packets that have addresses associated with that packet application module. A packet application module listens for its header,	collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64. "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is

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		e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the 'multiple-access packet channel.' In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the 'multiple-access packet channel,' and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an 'access window' of time, corresponding to a 'bit time-slot' on the TDM bus, to either capture the 'multiple-access packet channel' for transmission, or defer and allow the 'access window' to advance to the next packet application module in order. Once granted access,	assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; s*ee also* 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. Prior art discussion: "It should be understood that the network interface bandwidth is "channelized" and, in the context of packet data, expects a single multiplexed packet stream. NAU 100 is representative of a mixed TDM and packet NAU

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		that packet application module has sole access to the 'multiple-access packet channel' for a period of time, referred to herein as the 'access period.' During this 'access period,' a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the 'access window' is frozen at the current packet application module and does not advance until that packet application module releases the 'multiple-access packet channel.' Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the 'multiple-access packet channel.' In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several 'bit time-slots,' or clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and 'bit time-slots.' This	architecture. In this approach, NAU 100 provides a TDM bus in conjunction with one or more packet buses which taken together provide more bandwidth than is required to support the network interface. This additional bandwidth is used to support multiple point-to-point packet connections. Packet manager 110 not only aggregates the packet data, as mentioned above, but also allocates a fixed amount of the TDM bandwidth to the packet application modules." 1:51-64. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:4-10. "Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172. Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single

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		implied numbering is hereafter referred to as an 'ID number.' Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the 'bit time-slot' matches the ID number of the packet application module. In a system with N packet application modules, each 'bit time-slot' of the 'multiple-access packet channel' is counted in a repeating sequence from 0 to N-1 starting at some arbitrary 'bit time-slot' by each packet application module. In other words, each packet application module only counts those 'bit time-slots' assigned to the 'multiple-access packet channel.' The value of the count is the ID number for the 'bit time-slot.' All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a priori, the time-slots associated with the 'multiple-access packet channel.' In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a 'software-controlled' configuration, e.g., a	multiplexed packet stream." 2:21-27. FIGS. 3-8C *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of 'bit time-slots' may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts 'bit time-slots' of the 'multiple-access packet channel' beginning with 'bit time-slot' 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the 'bit time-slot' to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count	

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		equaling 0, which, in this example, occurs in 'bit time-slot' 1 of time-slot 1 of frame 1, 'bit time-slot' 8 of time-slot 1 of frame 1, 'bit time-slot' 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those 'bit time-slots' assigned to the 'multiple-access packet channel.' The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the 'bit time-slot' of the 'multiple-access packet channel,' i.e., the value of the count. The next two rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the 'bit time-slot' ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ	

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		signal whenever the ID numbers of the 'bit time-slot' and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the 'bit time-slot' and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next 'bit time-slot,' t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-	

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		slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of	

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		the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an 'initialize subroutine'(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and	

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		determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer	

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		315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the 'access window' in step 525. Once the 'access window' matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the 'bit time-slot' ID number, TDM/packet interface 310 asserts the PREQ signal in step 530. In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the	

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		PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the 'multiple-access packet channel' continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the 'multiple-access packet channel.' Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the 'multiple-access packet channel,' it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port.	

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		For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42.	
21. where the plurality of	7(e), 8, 9(d), 10,	Rembrandt does not believe this term requires construction. In the alternative: where more than	without the need for a central packet manager, each packet data source treats the second portion of the

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packet data sources share the second portion of the predefined bandwidth for transmitting packet data	11(d)	one source of packet data may use the second portion of predefined bandwidth [defined above] to transmit packet data [defined above]. Intrinsic Support: Abstract; FIGS. 6 & 8, "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In a feature of the invention, a contention scheme for accessing the "multiple-access packet channel" is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3;	predefined bandwidth as a single channel by contending for use of the entire channel in which no time slot is assigned to any particular packet data source *See row 20 above* Intrinsic Support: "I have realized an alternative approach to the design of TDM-based equipment . . . In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:40-48. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all

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		"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules." 4:56-5:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module	of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer

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		"grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access	315, and packet/TDM interface 310." 3:51-67. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is <u>shared</u> among at least two of the packet application modules. <u>This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module.</u> The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. <u>In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules.</u> (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, <u>this approach makes the entire</u>

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		packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." During this "access period," a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the "access	network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "As such, the starting point of a packet may lie anywhere in the 'multiple access packet channel.'" 5:47-52. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "Any method used for implementing a 'multiple-access packet channel' should be designed to achieve as close to 100% bandwidth efficient as possible. . . ." 6:26-32 "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous

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		window" is frozen at the current packet application module and does not advance until that packet application module releases the "multiple-access packet channel." Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the "multiple-access packet channel." In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several "bit time-slots," or clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module. In	property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64. "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38.

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		a system with N packet application modules, each "bit time-slot" of the "multiple-access packet channel" is counted in a repeating sequence from 0 to N-1 starting at some arbitrary "bit time-slot" by each packet application module. In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." The value of the count is the ID number for the "bit time-slot." All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a priori, the time-slots associated with the "multiple-access packet channel." In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged	"To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; s*ee also* 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42.

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		into. Note, this counting of "bit time-slots" may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts "bit time-slots" of the "multiple-access packet channel" beginning with "bit time-slot" 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the "bit time-slot" to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in "bit time-slot" 1 of time-slot 1 of frame 1, "bit time-slot" 8 of time-slot 1 of frame 1, "bit time-slot" 7 of	Prior art discussion: "It should be understood that the network interface bandwidth is "channelized" and, in the context of packet data, expects a single multiplexed packet stream. NAU 100 is representative of a mixed TDM and packet NAU architecture. In this approach, NAU 100 provides a TDM bus in conjunction with one or more packet buses which taken together provide more bandwidth than is required to support the network interface. This additional bandwidth is used to support multiple point-to-point packet connections. Packet manager 110 not only aggregates the packet data, as mentioned above, but also allocates a fixed amount of the TDM bandwidth to the packet application modules." 1:51-64. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:4-10. "Each packet application module communicates data

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		time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are "packet request" (PREQ) and "packet hold" (PHOLD). It is assumed these signals are bussed among the packet application modules as simply "open collector" as known in the art which allows them to be logically "OR"ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those "bit time-slots" assigned to the "multiple-access packet channel." The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the "bit time-slot" of the "multiple-access packet channel," i.e., the value of the count. The next two rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the "bit time-slot" ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the "bit time-	to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172. Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:21-27. FIGS. 3-8C *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		slot" and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the "bit time-slot" and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next "bit time-slot," t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-	

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		slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data.

It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 | |

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		drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B),	

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		and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the "multiple-access packet channel." The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER	

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		FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the "access window" in step 525. Once the "access window" matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the "bit time-slot" ID number, TDM/packet interface 310 asserts the PREQ signal in step 530. In step 535, TDM/packet interface 310 waits until	

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		PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the "multiple-access packet channel" continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the "multiple-access packet channel." Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size	

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		or number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues	

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		transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42	
22. in such a way that the allocated portion is shared among the plurality of packet data sources	15(c)	Rembrandt does not believe this term requires construction. In the alternative: in a manner so that only one source of packet data [defined above] should use any particular allotted time slot at any time. Intrinsic Support: Abstract; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus	without the need for a central packet manager, each packet data source treats the allocated portion as a single channel by contending for the entire channel in which no time slot is assigned to any particular packet data source *See row 20 above* Intrinsic Support: "I have realized an alternative approach to the design of TDM-based equipment . . . In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:40-48. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-

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		to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel."	access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented

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		In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. 5:11-42;	by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched

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		"The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources."6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17; z' The present invention relates to data communications, and more particularly, to communications systems that have channelized	(or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "As such, the starting point of a packet may lie anywhere in the 'multiple access packet channel.'" 5:47-52. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "Any method used for implementing a 'multiple - access packet channel' should be designed to achieve

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		network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56	as close to 100% bandwidth efficient as possible. . . ." 6:26-32 "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64. "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application

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			module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; s*ee also* 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet

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			interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. Prior art discussion: "It should be understood that the network interface bandwidth is "channelized" and, in the context of packet data, expects a single multiplexed packet stream. NAU 100 is representative of a mixed TDM and packet NAU architecture. In this approach, NAU 100 provides a TDM bus in conjunction with one or more packet buses which taken together provide more bandwidth than is required to support the network interface. This additional bandwidth is used to support multiple point-to-point packet connections. Packet manager 110 not only aggregates the packet data, as mentioned above, but also allocates a fixed amount of the TDM bandwidth to the packet application modules." 1:51-64. "For example, once the packet application modules exceed their allocated network interface bandwidth,

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			packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:4-10. "Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172. Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:21-27. FIGS. 3-8C *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance
23. allocating a portion of the bandwidth of the time-division multiplexed bus	20(b), 26	Rembrandt does not believe this term requires construction. In the alternative: allocating a portion of the bandwidth [defined above] to be accessed and shared by multiple sources of packet	without the need for a central packet manager, each packet data source treats the allocated portion as a single channel by contending for the entire channel in which no time slot is assigned to any particular

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as a multiple-access packet channel		data. Intrinsic Support: Abstract; FIGS. 6-8 C; FIGS. 3 & 4, element 204; FIGS. 5 & 7; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet	packet data source Intrinsic Support: "I have realized an alternative approach to the design of TDM-based equipment . . . In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:40-48. "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:53-57. "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet

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		application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the	manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a

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		art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules." 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the	"multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "As such, the starting point of a packet may lie

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		"outbound" TDM is similarly used for status and control information." 4:25-36; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a 'multiple-access packet channel' with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the 'multiple-access packet channel' for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the	anywhere in the 'multiple access packet channel.'" 5:47-52. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "Any method used for implementing a 'multiple - access packet channel' should be designed to achieve as close to 100% bandwidth efficient as possible. . . ." 6:26-32 "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this

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		network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The 'multiple-access packet channel' in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the 'multiple-access packet channel.' An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a 'bit time-slot.' It should be noted that the term 'time-slot' refers to a collection of 'bit time-slots.' Time-slots 1-6 represent the 'multiple-access packet channel.' As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and	embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64. "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8. "In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet

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		end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of 'bit time-slots' within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with 'bit time-slot' 7 in time-slot 4, of frame 1, and ends with 'bit time-slot 3' in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:20-6:5; "In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as	application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; s*ee also* 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. Prior art discussion: "It should be understood that the network interface bandwidth is "channelized" and, in the context of packet data, expects a single multiplexed packet stream. NAU 100 is representative of a mixed TDM and packet NAU architecture. In this approach, NAU 100 provides a

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		mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:43-6:5; "Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus	TDM bus in conjunction with one or more packet buses which taken together provide more bandwidth than is required to support the network interface. This additional bandwidth is used to support multiple point-to-point packet connections. Packet manager 110 not only aggregates the packet data, as mentioned above, but also allocates a fixed amount of the TDM bandwidth to the packet application modules." 1:51-64. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:4-10. "Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172. Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:21-27.

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		204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:52-64; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use	FIGS. 3-8C *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17	
_24._ distributed packet manager	1(d), 7(f), 8, 10, 15(e), 20(d), 26	A device, process or algorithm located within each packet data source, that controls how the packet data source accesses the time-division multiplexed bus. Intrinsic Support: Abstract; FIG. 3, elements 216-1, …, 216-N; FIG. 4, PACKET MANAGER; FIG. 6; FIG. 8; "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the	component within each packet data source that permits it to share the allotted bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time Intrinsic Support: Figs. 1-8C "In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:45-48. "This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:55-58. "This invention provides the following advantages:

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		network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service. In a feature of the invention, a contention scheme for accessing the "multiple-access packet channel" is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags. This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency; there is no additional overhead required for packet addressing on the bus; packet buffering is distributed across the bus, rather than being fixed in a central location; and the system has "modularity" and can quickly grow simply by adding additional packet application modules." 2:53-3:12; In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data	no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet

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		terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an "application specific integrated circuit" (ASIC), which is a programmable large-scale integrated circuit device that is dedicated to performing a specific function, or application, which in this case is described below. Packet interface processor 305 communicates packet data between packet/TDM interface 310 and line 304. The latter is representative of any one of a number of facilities for coupling packet application module 215-n to a packet system. For example, line 304 could be a local area network, or a dedicated	application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; see also 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever

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		facility to a "router" or a packet data terminal. Packet interface processor 305 performs packet handling, e.g., it provides the physical and link layer connections for packet transmission as known in the art, e.g., it checks for addresses, errors, etc., on the packets. Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309. It is assumed that lines 307 and 309 are representative of wideband data buses as known in the art. In the other direction, packet data from a far-end packet endpoint is received by packet interface processor 305 from packet/TDM interface 310 via line 306. Packet interface processor 305 receives a BUFFER FULL signal via line 314 from buffer 315, which provides a BUFFER NOT EMPTY signal via line 321 to packet/TDM interface 310. In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the	the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204." 4:25-28. "This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:61-62. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14. "Once granted access, that packet application module

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		network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and control information." 3:51-4:36; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet	has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 7:5-7 "To implement this slotted-access method two additional signals are bussed between packet application modules." 8:8-9. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal." 10:31-33. "Neither Calvignac nor Hogg teach a distributed packet manager as claimed by the present invention. …. Specifically, Hogg teaches a central manager which parcels access among packet data sources requiring a central device to accomplish the tasks of the central manager. This additional structure necessitates additional cost to assemble and operate, unlike the packet management of the instant invention which exists within each packet data source." Response 8/4/97 at p. 12; *See also* 4/4/97 Office Action "The prior art does not teach a distributed packet manager configured to allocate access to the allotted

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		channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:56-5:10; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As	bandwidth, within each packet data source." Examiner's Statement of Reasons for Allowance 10/1/97. Prior Art discussion in specification: "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:38-48. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:5-10. "Another prior art approach is illustrated in FIG. 2, which is similar to FIG. 1 except that separate point-to-point wideband packet buses have been replaced with separate TDM channels between each packet application module and the packet manager." 2:15-

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		described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as	19. "In particular, packet application modules 165-1 to 165-n are coupled to TDM bus 154, along with packet manager 170. Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:19-23. "Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:24-27. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted. As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application	

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		module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules. The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources. Any method used for implementing a "multiple-access packet channel" should be designed to achieve as close to 100% bandwidth efficiency as possible with no negative throughput effects due to congestion. The method should also have no inherent priority bias among the packet sources so that priorities may be enforced selectively if needed, preferably in software on the packet application modules. These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are	

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		contending for a fixed network pipe. Inbound packet data is already multiplexed as a single packet stream within the network channel. Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction. In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous	

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		property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 5:20-6:64; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-15; "In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is	

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		assumed that each packet application module is monitoring, or listening to, the 'multiple-access packet channel' for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an 'access window' of time,	

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		corresponding to a 'bit time-slot' on the TDM bus, to either capture the 'multiple-access packet channel' for transmission, or defer and allow the 'access window' to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the 'multiple-access packet channel' for a period of time, referred to herein as the 'access period.' During this 'access period,' a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the 'access window' is frozen at the current packet application module and does not advance until that packet application module releases the 'multiple-access packet channel.' Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the 'multiple-access packet channel.' In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several 'bit time-slots,' or clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission,	

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		avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module. In a system with N packet application modules, each "bit time-slot" of the "multiple-access packet channel" is counted in a repeating sequence from 0 to N-1 starting at some arbitrary 'bit time-slot' by each packet application module. In other words, each packet application module only counts those 'bit time-slots' assigned to the 'multiple-access packet channel.' The value of the count is the ID number for the 'bit time-slot.' All packet application modules are synchronized with this counting sequence and are aware of the ID number of each 'bit time-slot' at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a priori, the time-slots associated with the 'multiple-access packet channel.' In combination with this,	

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		each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a 'software-controlled' configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of 'bit time-slots' may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts 'bit time-slots' of the 'multiple-access packet channel' beginning with 'bit time-slot' 1 of frame 1, which is associated with the count value of 0. Each packet application	

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		module waits for its ID number to equal the count, or ID number, of the "bit time-slot" to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in 'bit time-slot' 1 of time-slot 1 of frame 1, 'bit time-slot' 8 of time-slot 1 of frame 1, 'bit time-slot' 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed. Referring back to FIG. 6, a sequence of 'bit time-slots' is shown. This sequence of bit time-slots only represents those 'bit time-slots' assigned to the 'multiple-access packet channel.' The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the 'bit time-slot' of the 'multiple-access packet channel,' i.e., the value of the count. The next two rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet	

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		data. Beginning at time t2, the "bit time-slot" ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the 'bit time-slot' and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the "bit time-slot" and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next "bit time-slot," t6, packet application module 2 concatenates its packet stream with that of the previous	

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		transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in accordance with HDLC, the last packet application module	

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		may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different 'subroutines' for	

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		simplicity, i.e., an "initialize subroutine"(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each 'bit time-slot' of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly	

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		back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the "access window" in step 525. Once the "access window" matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the "bit time-slot" ID number, TDM/packet interface 310 asserts the PREQ signal in step 530. In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting	

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		the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the 'multiple-access packet channel' continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the 'multiple-access packet channel.' Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the 'multiple-access packet channel,' it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement	

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		rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to	

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		allow another packet application module to gain access to the TDM bus." 6:41-10:42; "In addition, although illustrated in the context of a T1 network facility, the inventive concept applies to other network facilities as well, e.g., fractional T1, digital data service (DDS), T3, etc. Further, more than one "multiple-access packet channel," can exist. For example, a first plurality of packet application modules may be assigned to a first group of time-slots, e.g., time-slots 1-6, for transmitting packet data, while a second plurality of packet application modules is assigned to a second group of time-slots, e.g., time-slots 7-12, for transmitting packet data. Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:3-16;	
25. wherein each one of the plurality of	10, 11(d)	Rembrandt does not believe this term requires construction. In the alternative: each of the multiple sources of packet data [defined above] is	circuitry within each packet data source that permits them to share the second portion of the predefined bandwidth, without the need for a centralized packet

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packet data sources includes interface circuitry to the time division multiplexed bus for synchronizing packet data to the time division multiplexed bus		operatively connected to the time division multiplexed bus [defined above] using interface circuitry in a manner that allows packet data to be communicated from that source of packet data within an appropriate allotted time slot for that source of packet data. Intrinsic Support: Abstract; FIG 4, element 310; "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the	manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time Intrinsic Support: "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus;" 3:3-8 "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206." 4:25-31. FIGS. 4; 5-8C *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See row 24 above*

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		asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 3:48-51; "A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310. The latter is an "application specific integrated circuit" (ASIC), which is a programmable large-	

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		scale integrated circuit device that is dedicated to performing a specific function, or application, which in this case is described below. Packet interface processor 305 communicates packet data between packet/TDM interface 310 and line 304. The latter is representative of any one of a number of facilities for coupling packet application module 215-n to a packet system. For example, line 304 could be a local area network, or a dedicated facility to a "router" or a packet data terminal. Packet interface processor 305 performs packet handling, e.g., it provides the physical and link layer connections for packet transmission as known in the art, e.g., it checks for addresses, errors, etc., on the packets. Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309. It is assumed that lines 307 and 309 are representative of wideband data buses as known in the art. In the other direction, packet data from a far-end packet endpoint is received by packet interface processor 305 from packet/TDM interface 310 via line 306. Packet interface processor 305 receives a BUFFER FULL signal via line 314 from buffer 315, which provides a BUFFER NOT EMPTY signal via line	

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		321 to packet/TDM interface 310. In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and control information. The storage size of buffer 315 is determined empirically and is a function of the type of packet equipment and its data rate. For example, if a packet application module is interfacing to a router, as known in the art, a router may communicate packet data on the order of 128 Kb/sec. Consequently if the packet application module cannot, for the moment, transmit a packet from the router to the TDM bus, the packet application module can perform flow control with the router with a concomitant minimal amount of buffering required on the packet application module because	

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		of the low data rate from the router. Conversely, if a packet application module is interfacing to a LAN, which typically communicates data at a higher speed, e.g., 10 Mb/sec., a larger amount of buffering may be required on the packet application module. Thus, depending on the packet equipment, each packet application module may have different buffering requirements--but each packet application module has less buffer requirements than the packet manager module of the prior art." 3:61-4:55; FIGS. 6 & 8	
26. controlling access by said packet data sources to the allocated portion of the bandwidth via a distributed packet manager within each of said packet data sources	15(e), 20(d), 26	Rembrandt does not believe this term requires construction. In the alternative: each source of packet data using a distributed packet manager [defined above] within that source of packet data to control that source's access to an allocated portion of the bandwidth [defined above]. Intrinsic Support: "The present invention relates to data communications, and more particularly, to communications systems that have channelized network access, and may transport both	using a component within each packet data source that permits them to share the allocated portion of the bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at a time Intrinsic Support: Figs. 1-8C "In particular, multiple packet data sources share a

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		synchronous data and variable-bit-rate data such as frame relay (hereafter referred to as packet data), in a time-division multiplexed format." 1:6-11; "To provide the most flexibility, it is preferable that the NAU support two types of data: synchronous data and packet data. For example, the support of synchronous data provides the ability to make telephone, i.e., voice, calls, while the support of packet data provides the ability to interwork with public network packet services. However, the asynchronous nature of packet data at the logical level combined with the requirements of synchronous data causes design tradeoffs in both the complexity and cost of an NAU." 1:17-26; "Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated." 3:53-56; Abstract; FIG. 3, elements 216-1, …, 216-N; FIG. 4, PACKET MANAGER; FIG. 6; FIG. 8; "In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet	single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:45-48. "This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:55-58. "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now

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		application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet application module includes its own TDM bus interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service.

In a feature of the invention, a contention scheme for accessing the "multiple-access packet channel" is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags.

This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency; there is no additional overhead required for packet | distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules.

A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67.

"To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; see also 8:24-9:17

"The only hardware function required to support such |

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		addressing on the bus; packet buffering is distributed across the bus, rather than being fixed in a central location; and the system has "modularity" and can quickly grow simply by adding additional packet application modules." 2:53-3:12, "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor	strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204." 4:25-28. "This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:61-62. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet

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		305, buffer 315, and packet/TDM interface 310. The latter is an "application specific integrated circuit" (ASIC), which is a programmable large-scale integrated circuit device that is dedicated to performing a specific function, or application, which in this case is described below. Packet interface processor 305 communicates packet data between packet/TDM interface 310 and line 304. The latter is representative of any one of a number of facilities for coupling packet application module 215-n to a packet system. For example, line 304 could be a local area network, or a dedicated facility to a "router" or a packet data terminal. Packet interface processor 305 performs packet handling, e.g., it provides the physical and link layer connections for packet transmission as known in the art, e.g., it checks for addresses, errors, etc., on the packets. Packet data transmitted to a far-end packet endpoint is provided from packet interface processor 305 to packet/TDM interface 310 via line 307, buffer 315, and line 309. It is assumed that lines 307 and 309 are representative of wideband data buses as known in the art. In the other direction, packet data from a far-end packet endpoint is received by packet interface processor 305 from packet/TDM interface 310 via line 306.	application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14. "Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 7:5-7 "To implement this slotted-access method two additional signals are bussed between packet application modules." 8:8-9. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal." 10:31-33. "Neither Calvignac nor Hogg teach a distributed packet manager as claimed by the present invention. .... Specifically, Hogg teaches a central manager which parcels access among packet data sources requiring a central device to accomplish the tasks of

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		Packet interface processor 305 receives a BUFFER FULL signal via line 314 from buffer 315, which provides a BUFFER NOT EMPTY signal via line 321 to packet/TDM interface 310. In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and control information." 3:51-4:36; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed	the central manager. This additional structure necessitates additional cost to assemble and operate, unlike the packet management of the instant invention which exists within each packet data source." Response 8/4/97 at p. 12; *See also* 4/4/97 Office Action "The prior art does not teach a distributed packet manager configured to allocate access to the allotted bandwidth, within each packet data source." Examiner's Statement of Reasons for Allowance 10/1/97. Prior Art discussion in specification: "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:38-48. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of

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		fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:56-5:10; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the	considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:5-10. "Another prior art approach is illustrated in FIG. 2, which is similar to FIG. 1 except that separate point-to-point wideband packet buses have been replaced with separate TDM channels between each packet application module and the packet manager." 2:15-19. "In particular, packet application modules 165-1 to 165-n are coupled to TDM bus 154, along with packet manager 170. Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:19-23. "Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:24-27. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of

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		full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-15; "In the context of this invention, it is assumed that all modules are continually listening to the TDM in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the "multiple-access packet channel" for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to	Allowance

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		implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." During this "access period," a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the "access window" is frozen at the current packet application module and does not advance until that packet	

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		application module releases the "multiple-access packet channel." Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the "multiple-access packet channel." In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several "bit time-slots," or clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module. In a system with N packet application modules, each "bit time-slot" of the "multiple-access packet	

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		channel" is counted in a repeating sequence from 0 to N-1 starting at some arbitrary "bit time-slot" by each packet application module. In other words, each packet application module only counts those "bit time-slots" assigned to the "multiple-access packet channel." The value of the count is the ID number for the "bit time-slot." All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a priori, the time-slots associated with the "multiple-access packet channel." In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a "software-controlled" configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of "bit time-slots" may span more than one frame. Since N may be any	

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		integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts "bit time-slots" of the "multiple-access packet channel" beginning with "bit time-slot" 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the "bit time-slot" to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in "bit time-slot" 1 of time-slot 1 of frame 1, "bit time-slot" 8 of time-slot 1 of frame 1, "bit time-slot" 7 of time-slot 2 of frame 1 etc.	

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		To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are "packet request" (PREQ) and "packet hold" (PHOLD). It is assumed these signals are bussed among the packet application modules as simply "open collector" as known in the art which allows them to be logically "OR"ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those "bit time-slots" assigned to the "multiple-access packet channel." The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the "bit time-slot" of the "multiple-access packet channel," i.e., the value of the count. The next two rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the "bit time-slot" ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the "bit time-slot" and the packet application module match. Upon receiving the PREQ signal, each packet	

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		application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the "bit time-slot" and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next "bit time-slot," t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application	

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		module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished.	

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		As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an "initialize subroutine"(FIG. 8A), "request to transmit a packet subroutine" (FIG. 8B), and a "wait for PHOLD" subroutine (FIG. 8C). In step 505, packet application module 215-n is	

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		initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the "multiple-access packet channel." The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value.

When there is a packet to transmit, packet interface processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet | |

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		interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the "access window" in step 525. Once the "access window" matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the "bit time-slot" ID number, TDM/packet interface 310 asserts the PREQ signal in step 530. In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o.	

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		Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the "multiple-access packet channel" continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the "multiple-access packet channel." Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the "multiple-access packet channel," it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or number of packets sent during one access period, the application software is then able to implement	

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		rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the	

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		TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42	
27. allocate access to the allotted bandwidth among said packet data sources	1	Control access by each of the packet data [defined above] sources to a portion of the bandwidth previously assigned to packet data [defined above]. Intrinsic Support: Abstract; FIGS. 6-8 C; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In a feature of the invention, a contention scheme	component within each packet data source that permits it to share the allotted bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time Intrinsic Support: Figs. 1-8C "In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:45-48. "This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:55-58.

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		for accessing the 'multiple-access packet channel' is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the 'multiple-access packet channel' with the other packet application	"This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the

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		modules." 4:56-5:5; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a 'multiple-access packet channel' with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the 'multiple-access packet channel' for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e.,	inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; see also 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown)

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		NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The 'multiple-access packet channel' in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the 'multiple-access packet channel.' An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a 'bit time-slot.' It should be noted that the term 'time-slot' refers to a collection of 'bit time-slots.' Time-slots 1-6 represent the 'multiple-access packet channel.' As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each	is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204." 4:25-28. "This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:61-62. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14.

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		packet is mapped into a plurality of 'bit time-slots' within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with 'bit time-slot' 7 in time-slot 4, of frame 1, and ends with 'bit time-slot 3' in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:20-6:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM	"Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 7:5-7 "To implement this slotted-access method two additional signals are bussed between packet application modules." 8:8-9. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal." 10:31-33. "Neither Calvignac nor Hogg teach a distributed packet manager as claimed by the present invention. …. Specifically, Hogg teaches a central manager which parcels access among packet data sources requiring a central device to accomplish the tasks of the central manager. This additional structure necessitates additional cost to assemble and operate, unlike the packet management of the instant invention which exists within each packet data source." Response 8/4/97 at p. 12; *See also* 4/4/97 Office Action "The prior art does not teach a distributed packet

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		in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the 'multiple-access packet channel' for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the 'multiple-access packet channel.' In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the 'multiple-access packet channel,' and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-	manager configured to allocate access to the allotted bandwidth, within each packet data source." Examiner's Statement of Reasons for Allowance 10/1/97. Prior Art discussion in specification: "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:38-48. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:5-10. "Another prior art approach is illustrated in FIG. 2, which is similar to FIG. 1 except that separate point-to-point wideband packet buses have been replaced with separate TDM channels between each packet

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		access method, each packet application module, in rotation order, is given an 'access window' of time, corresponding to a 'bit time-slot' on the TDM bus, to either capture the 'multiple-access packet channel' for transmission, or defer and allow the 'access window' to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the 'multiple-access packet channel' for a period of time, referred to herein as the 'access period.' During this 'access period,' a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the 'access window' is frozen at the current packet application module and does not advance until that packet application module releases the 'multiple-access packet channel.' Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the 'multiple-access packet channel.' In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several 'bit time-slots,' or	application module and the packet manager." 2:15-19. "In particular, packet application modules 165-1 to 165-n are coupled to TDM bus 154, along with packet manager 170. Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:19-23. "Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:24-27. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and 'bit time-slots.' This implied numbering is hereafter referred to as an 'ID number.' Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the 'bit time-slot' matches the ID number of the packet application module. In a system with N packet application modules, each 'bit time-slot' of the 'multiple-access packet channel' is counted in a repeating sequence from 0 to N-1 starting at some arbitrary 'bit time-slot' by each packet application module. In other words, each packet application module only counts those 'bit time-slots' assigned to the 'multiple-access packet channel.' The value of the count is the ID number for the 'bit time-slot.' All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a	

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		priori, the time-slots associated with the 'multiple-access packet channel.' In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a 'software-controlled' configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of 'bit time-slots' may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts 'bit time-slots' of the 'multiple-access packet channel' beginning with	

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		'bit time-slot' 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the 'bit time-slot' to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in 'bit time-slot' 1 of time-slot 1 of frame 1, 'bit time-slot' 8 of time-slot 1 of frame 1, 'bit time-slot' 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those 'bit time-slots' assigned to the 'multiple-access packet channel.' The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the 'bit time-slot' of the 'multiple-access packet channel,' i.e., the value of the count. The next two	

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		rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the 'bit time-slot' ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the 'bit time-slot' and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the 'bit time-slot' and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next 'bit time-slot,'	

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		t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus 204-o to insert data. In addition, and in	

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		accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4	

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		is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an 'initialize subroutine'(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface	

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		processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the 'access window' in step 525. Once the 'access window' matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the 'bit time-slot' ID number, TDM/packet interface 310 asserts the PREQ signal in step 530.	

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		In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the 'multiple-access packet channel' continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the 'multiple-access packet channel.' Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the 'multiple-access packet channel,' it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or	

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		number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the	

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		TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42.	
28. allocate access to the second portion of the predefined bandwidth among said packet data sources	7	Control access by each of the packet data [defined above] sources to a portion of the predefined bandwidth [defined above].

Intrinsic Support:

Abstract; FIGS. 6-8 C;

"In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57;

"In a feature of the invention, a contention scheme | component within each packet data source that permits it to share the allotted bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time

Intrinsic Support:

Figs. 1-8C

"In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data." 2:45-48.

"This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:55-58. |

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		for accessing the 'multiple-access packet channel' is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3;

"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the 'multiple-access packet channel' with the other packet application | "This invention provides the following advantages: no central packet manager is required to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8

"In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61

"In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules.

A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the |

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		modules." 4:56-5:5; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a 'multiple-access packet channel' with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the 'multiple-access packet channel' for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e.,	inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; see also 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown)

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		NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The 'multiple-access packet channel' in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the 'multiple-access packet channel.' An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a 'bit time-slot.' It should be noted that the term 'time-slot' refers to a collection of 'bit time-slots.' Time-slots 1-6 represent the 'multiple-access packet channel.' As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each	is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42.

"In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204." 4:25-28.

"This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:61-62.

"As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14. |

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		packet is mapped into a plurality of 'bit time-slots' within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with 'bit time-slot' 7 in time-slot 4, of frame 1, and ends with 'bit time-slot 3' in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:20-6:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM	"Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 7:5-7 "To implement this slotted-access method two additional signals are bussed between packet application modules." 8:8-9. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal." 10:31-33. "Neither Calvignac nor Hogg teach a distributed packet manager as claimed by the present invention. …. Specifically, Hogg teaches a central manager which parcels access among packet data sources requiring a central device to accomplish the tasks of the central manager. This additional structure necessitates additional cost to assemble and operate, unlike the packet management of the instant invention which exists within each packet data source." Response 8/4/97 at p. 12; *See also* 4/4/97 Office Action "The prior art does not teach a distributed packet

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		in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the 'multiple-access packet channel' for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the 'multiple-access packet channel.' In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the 'multiple-access packet channel,' and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-	manager configured to allocate access to the allotted bandwidth, within each packet data source." Examiner's Statement of Reasons for Allowance 10/1/97. Prior Art discussion in specification: "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:38-48. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:5-10. "Another prior art approach is illustrated in FIG. 2, which is similar to FIG. 1 except that separate point-to-point wideband packet buses have been replaced with separate TDM channels between each packet

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		access method, each packet application module, in rotation order, is given an 'access window' of time, corresponding to a 'bit time-slot' on the TDM bus, to either capture the 'multiple-access packet channel' for transmission, or defer and allow the 'access window' to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the 'multiple-access packet channel' for a period of time, referred to herein as the 'access period.' During this 'access period,' a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the 'access window' is frozen at the current packet application module and does not advance until that packet application module releases the 'multiple-access packet channel.' Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the 'multiple-access packet channel.' In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several 'bit time-slots,' or	application module and the packet manager." 2:15-19. "In particular, packet application modules 165-1 to 165-n are coupled to TDM bus 154, along with packet manager 170. Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:19-23. "Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:24-27. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and 'bit time-slots.' This implied numbering is hereafter referred to as an 'ID number.' Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the 'bit time-slot' matches the ID number of the packet application module. In a system with N packet application modules, each 'bit time-slot' of the 'multiple-access packet channel' is counted in a repeating sequence from 0 to N-1 starting at some arbitrary 'bit time-slot' by each packet application module. In other words, each packet application module only counts those 'bit time-slots' assigned to the 'multiple-access packet channel.' The value of the count is the ID number for the 'bit time-slot.' All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a	

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		priori, the time-slots associated with the 'multiple-access packet channel.' In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a 'software-controlled' configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of 'bit time-slots' may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts 'bit time-slots' of the 'multiple-access packet channel' beginning with	

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		'bit time-slot' 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the 'bit time-slot' to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in 'bit time-slot' 1 of time-slot 1 of frame 1, 'bit time-slot' 8 of time-slot 1 of frame 1, 'bit time-slot' 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those 'bit time-slots' assigned to the 'multiple-access packet channel.' The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the 'bit time-slot' of the 'multiple-access packet channel,' i.e., the value of the count. The next two	

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		rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the 'bit time-slot' ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the 'bit time-slot' and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the 'bit time-slot' and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next 'bit time-slot,'	

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		t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus	

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		204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4	

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		is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an 'initialize subroutine'(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface	

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		processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the 'access window' in step 525. Once the 'access window' matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the 'bit time-slot' ID number, TDM/packet interface 310 asserts the PREQ signal in step 530.	

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		In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the 'multiple-access packet channel' continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the 'multiple-access packet channel.' Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the 'multiple-access packet channel,' it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or	

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		number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the	

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		TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42.	
29. controlling [the] access by said packet data sources to the allocated portion of the bandwidth	15, 20	Controlling access by each of the packet data [defined above] sources to a the allocated portion of the bandwidth [defined below]. Intrinsic Support: Abstract; FIGS. 6-8 C; "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In a feature of the invention, a contention scheme	component within each packet data source that permits it to share the allotted bandwidth, without the need for a centralized packet manager, by communicating with other packet data sources to control which one of the plurality of packet data sources can attempt to access the allotted bandwidth at any one time Intrinsic Support: Figs. 1-8C "In particular, multiple packet data sources share a single TDM channel. As a result, <u>no central packet manager is required</u> to aggregate the packet data." 2:45-48. "This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:55-58.

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		for accessing the 'multiple-access packet channel' is described that avoids packet collisions, maximizes bandwidth efficiency, and provides for interframe High-level Data Link Control (HDLC) flags." 2:66-3:3; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module**.** The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module must contend for the bandwidth of the 'multiple-access packet channel' with the other packet application	"This invention provides the following advantages: <u>no central packet manager is required</u> to synchronize packet data to the TDM bus; packet sources share all of the TDM bandwidth allocated to packet data resulting in maximum efficiency." 3:3-8 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and <u>the packet manager is eliminated</u> . . . ." 3:51-61 "<u>In accordance with the inventive concept, multiple packet application modules now share a single TDM channel</u> (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the

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		modules." 4:56-5:5; "In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a 'multiple-access packet channel' with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the 'multiple-access packet channel' for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e.,	inventive concept, the components of packet application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed.. . . . The next two rows represent the state of the PREQ and PHOLD busses." 8:8-23; see also 8:24-9:17 "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown)

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		NAM 205 is not required to buffer the packet data. In accordance with a feature of the invention, it is assumed that packet transmission is utilizing HDLC, which is a bit-oriented layer 2 protocol that produces variable bit length packets. This allows a packet to be spread across time-slots and multiple TDM frames. The 'multiple-access packet channel' in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the 'multiple-access packet channel.' An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a 'bit time-slot.' It should be noted that the term 'time-slot' refers to a collection of 'bit time-slots.' Time-slots 1-6 represent the 'multiple-access packet channel.' As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each	is received by the TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 10:31-42. "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204." 4:25-28. "This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:61-62. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14.

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		packet is mapped into a plurality of 'bit time-slots' within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5, where packet 50 begins with 'bit time-slot' 7 in time-slot 4, of frame 1, and ends with 'bit time-slot 3' in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:20-6:5; "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth. However, if a packet application module cannot "grab" the "multiple-access packet channel," then that packet application module must queue, or buffer, the packet. As a result, the flow control is now distributed among the packet application modules." 6:6-14; "In the context of this invention, it is assumed that all modules are continually listening to the TDM	"Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period." 7:5-7 "To implement this slotted-access method two additional signals are bussed between packet application modules." 8:8-9. "The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal." 10:31-33. "Neither Calvignac nor Hogg teach a distributed packet manager as claimed by the present invention. …. Specifically, Hogg teaches a central manager which parcels access among packet data sources requiring a central device to accomplish the tasks of the central manager. This additional structure necessitates additional cost to assemble and operate, unlike the packet management of the instant invention which exists within each packet data source." Response 8/4/97 at p. 12; *See also* 4/4/97 Office Action "The prior art does not teach a distributed packet

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		in-bound bus to pull off data addressed to them. In the case of the packet application modules, it is assumed that each packet application module is monitoring, or listening to, the 'multiple-access packet channel' for packets that have addresses associated with that packet application module. A packet application module listens for its header, e.g., virtual address, if it is not their packet, it is just dropped. The remainder of this description will focus on outbound packet traffic. In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the 'multiple-access packet channel.' In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the 'multiple-access packet channel,' and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module. Before describing it in detail, an overview of this slotted-access method is described. In the slotted-	manager configured to allocate access to the allotted bandwidth, within each packet data source." Examiner's Statement of Reasons for Allowance 10/1/97. Prior Art discussion in specification: "The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104. The packet application modules couple packet data equipment (not shown), e.g., a data terminal, to packet manager 110." 1:38-48. "For example, once the packet application modules exceed their allocated network interface bandwidth, packet manager 110 must take steps to prevent the loss of any packet data. These steps include buffering the packet data, which may require a buffer of considerable size to support all of the packet application modules, and, perhaps, flow control to throttle the packet traffic." 2:5-10. "Another prior art approach is illustrated in FIG. 2, which is similar to FIG. 1 except that separate point-to-point wideband packet buses have been replaced with separate TDM channels between each packet

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		access method, each packet application module, in rotation order, is given an 'access window' of time, corresponding to a 'bit time-slot' on the TDM bus, to either capture the 'multiple-access packet channel' for transmission, or defer and allow the 'access window' to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the 'multiple-access packet channel' for a period of time, referred to herein as the 'access period.' During this 'access period,' a packet application module sends at least one HDLC frame of queued packet traffic toward the network, and the 'access window' is frozen at the current packet application module and does not advance until that packet application module releases the 'multiple-access packet channel.' Under some conditions however, a packet application module may not begin transmitting packet data as soon as it has captured the 'multiple-access packet channel.' In particular, whenever the previously transmitting packet application module is still transmitting a packet or closing flag, the next packet application module must wait until completion before transmitting its first packet. Since a rotational arbitration scheme on the bus may take several 'bit time-slots,' or	application module and the packet manager." 2:15-19. "In particular, packet application modules 165-1 to 165-n are coupled to TDM bus 154, along with packet manager 170. Each packet application module communicates data to, and from, packet manager 170 in a separate TDM channel as represented by lines 171 and 172." 2:19-23. "Like the description above for FIG. 1, packet manager 170 aggregates the packet traffic to NAM 155 via a TDM channel, as represented by line 173, to create a single multiplexed packet stream." 2:24-27. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		clock, intervals, this mechanism allows the arbitration to overlap an active packet transmission, avoiding idle time on the bus and increasing bandwidth utilization. FIG. 6 shows an illustrative slotted-access method. There is an implied numbering of the packet application modules and 'bit time-slots.' This implied numbering is hereafter referred to as an 'ID number.' Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the 'bit time-slot' matches the ID number of the packet application module. In a system with N packet application modules, each 'bit time-slot' of the 'multiple-access packet channel' is counted in a repeating sequence from 0 to N-1 starting at some arbitrary 'bit time-slot' by each packet application module. In other words, each packet application module only counts those 'bit time-slots' assigned to the 'multiple-access packet channel.' The value of the count is the ID number for the 'bit time-slot.' All packet application modules are synchronized with this counting sequence and are aware of the ID number of each "bit time-slot" at all times. As a result, the ID number need not be present on the bus. As noted earlier, each packet application module knows, a	

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		priori, the time-slots associated with the 'multiple-access packet channel.' In combination with this, each packet application module is configured with an unique ID number, which can be determined in any number of ways. For example, each module, or circuit board, can have an address associated either via a 'software-controlled' configuration, e.g., a system administer literally assigns addresses to the various modules; or by a hardware setting that specifically associates a particular address with a particular position in the system, e.g., what slot the circuit board is plugged into. Note, this counting of 'bit time-slots' may span more than one frame. Since N may be any integer there is no relationship between this ID numbering and the position of bits in the TDM frame. For example, if there are seven packet application modules, and assuming for the moment that none of the seven packet application modules wanted access to the TDM bus, this counting would look like that shown in FIG. 7. FIG. 7 is similar to FIG. 5, except packet 50 has been removed, i.e., there is no transmission of a packet and only time-slots 1 and 2 of frame 1 are shown. It is assumed that each packet application module counts 'bit time-slots' of the 'multiple-access packet channel' beginning with	

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		'bit time-slot' 1 of frame 1, which is associated with the count value of 0. Each packet application module waits for its ID number to equal the count, or ID number, of the 'bit time-slot' to attempt to access TDM bus 204-o. For example, the packet application module associated with ID 0, can attempt access only upon the value of the count equaling 0, which, in this example, occurs in 'bit time-slot' 1 of time-slot 1 of frame 1, 'bit time-slot' 8 of time-slot 1 of frame 1, 'bit time-slot' 7 of time-slot 2 of frame 1 etc. To implement this slotted-access method two additional signals are bussed between packet application modules. These signals are 'packet request' (PREQ) and 'packet hold' (PHOLD). It is assumed these signals are bussed among the packet application modules as simply 'open collector' as known in the art which allows them to be logically 'OR'ed. Referring back to FIG. 6, a sequence of "bit time-slots" is shown. This sequence of bit time-slots only represents those 'bit time-slots' assigned to the 'multiple-access packet channel.' The top row of FIG. 6 is simply a sequence of bit time reference points. The second row of FIG. 6 is the ID number of the 'bit time-slot' of the 'multiple-access packet channel,' i.e., the value of the count. The next two	

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		rows represent the state of the PREQ and PHOLD busses. The final row simply represents packet data. Beginning at time t2, the 'bit time-slot' ID number is equal to 0. In order for a packet application module to transmit a packet on TDM bus 204-o, the packet application module must assert the PREQ signal whenever the ID numbers of the 'bit time-slot' and the packet application module match. Upon receiving the PREQ signal, each packet application module halts the counting. The packet application module that asserted the PREQ signal becomes the next in line to begin transmission. For example, when the packet application module associated with the ID number of 2 wants to transmit, it must wait until time t4, when the ID numbers of the 'bit time-slot' and the packet application module match, to assert the PREQ signal. However, the presence of a PHOLD signal driven by the currently transmitting packet application module delays the access of packet application module 2 to TDM bus 204-o until PHOLD is withdrawn at time t5. (The question marks illustrated in FIG. 6 simply represent that another, unidentified packet application module is currently transmitting.) At the next 'bit time-slot,'	

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		t6, packet application module 2 concatenates its packet stream with that of the previous transmission. Although it could occur at any point, it is assumed that packet application module 2 drops the PREQ signal at the end of its packet transmission (described below) to allow the counting of time-slots by all packet application modules to again advance. At the same time, packet application module 2 asserts the PHOLD signal, which prevents the next packet application module from beginning its transmission until packet application module 2 has completed its closing flag sequence. These events occur at time t9. Subsequently, packet application module 6 raises it PREQ signal at time t13, signaling its readiness to send at least one packet, while packet application module 2 is still transmitting its closing flag. At time t18, packet application module 2 completes its packet transmission and drops PHOLD. At time t19, packet application module 6 begins sending its packet data. It should be noted that the HDLC flags are a byte in length. Consequently, transmission of an HDLC inter-frame flag must end first before another packet application module can get the TDM bus	

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		204-o to insert data. In addition, and in accordance with HDLC, the last packet application module may continue inserting the inter-frame flags, and asserting the PHOLD signal until the PREQ signal is asserted, by itself or another module. Once the PREQ signal is asserted, TDM/packet interface 310 drops the PHOLD signal only when the insertion of the current flag is finished. As mentioned above, the point at which an actively transmitting packet application module asserts the PHOLD signal and lowers the PREQ signal is arbitrary. The earlier this occurs, the higher the probability that the next packet application module will be found by the time the first closing flag sequence is sent. This increases the efficiency of the "multiple-access packet channel" because there is no waiting for data transmission to finish to start arbitration again, i.e., no time is lost for contention (a packet application module is always ready to go). On the other hand, waiting until near the end of the transmission allows more timely packet queue information to be used in the arbitration. A balance between these two extremes could be implemented. A method illustrating this slotted-access technique for use in the packet application module of FIG. 4	

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		is shown in FIG. 8. The steps shown in FIG. 8 have been divided into different "subroutines" for simplicity, i.e., an 'initialize subroutine'(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value. When there is a packet to transmit, packet interface	

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		processor 305 begins to fill buffer 315 provided buffer 315 is not full. In particular, referring briefly back to FIG. 4, it can be seen that a BUFFER FULL signal is provided by buffer 315 to packet interface processor 305. This signal alerts packet interface processor 305 if buffer 315 is full. As a result, packet interface processor 305 fills buffer 315 when packet data is available to transmit only if the BUFFER FULL signal is not active. Once the BUFFER FULL signal is active, packet interface processor 305 could, if necessary, perform flow-control, if possible, with the associated packet endpoint like a router, or simply begin dropping packets. Assuming buffer 315 is initially empty, as packet interface processor 305 begins to fill up buffer 315, the BUFFER NOT EMPTY signal is asserted for TDM/packet interface 310 in step 520, via line 321. Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the 'access window' in step 525. Once the 'access window' matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the 'bit time-slot' ID number, TDM/packet interface 310 asserts the PREQ signal in step 530.	

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		In step 535, TDM/packet interface 310 waits until PHOLD is no longer asserted before transmitting the packet from buffer 315 onto TDM bus 204-o. Upon nearing the end of the packet transmission (which can be determined simply by knowing the length of the packet from the packet header information), TDM/packet interface 310 drops the PREQ signal and asserts the PHOLD signal in step 540. As mentioned above, the last packet application module to grab the 'multiple-access packet channel' continues inserting flags and asserting PHOLD until PREQ is asserted, by itself or another module. Once PREQ is again asserted, TDM/packet interface 310 drops PHOLD only when the insertion of an flag is finished. At this point the next packet application module then has access to the 'multiple-access packet channel.' Within this general method, different approaches may be taken to offset the arbitration fairness. In general, each time a packet application module gains transmission access to the 'multiple-access packet channel,' it may send any prescribed number of packets. The access method may be designed to limit this number to one, or it may allow the application to empty its packet transmit buffer. If the hardware imposes no limit on the size or	

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		number of packets sent during one access period, the application software is then able to implement rules for sending varying amounts of packet traffic across the bus. There is no reason why those rules must be applied the same for every packet application module, and in fact could be different for each port. For example, the packet application module may send as many packets as can be transmitted within a fixed amount of time. Another possibility is that the amount of packet data transmitted may be a function of the number of packets queued or the time they have been queued. The size of the packets, always known to the software, may also be a factor in determining when to terminate the access period. The only hardware function required to support such strategies is the combination of the PREQ signal and PHOLD signal. Once the active packet application module is about to fulfill its prescribed transmission requirement, the corresponding packet interface processor either informs the respective TDM/packet interface via a control line (not shown) or the TDM/packet interface continues transmitting until a corresponding BUFFER EMPTY signal (not shown) is received by the	

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		TDM/packet interface. Whatever the signal, the TDM/packet interface then stops asserting PREQ to allow another packet application module to gain access to the TDM bus." 6:41-10:42.	
30. the second portion of the predefined bandwidth being shared in such a way that only one of the plurality of packet data sources accesses the second portion of the predefined bandwidth at a time	9(d)	Rembrandt does not believe this term requires construction. In the alternative: the second portion of the predefined bandwidth [defined above] is used by the sources of packet data so that only one source of packet data should use any particular allotted time slot at a time. Intrinsic Support: "In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57;	sharing where only one packet data source can attempt to access the predefined second portion at a time Intrinsic Support: FIGS. 4-8C "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8.

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		"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62;

"NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel."

In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple- | "There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module." 7:25-31.

"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module. The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added).

"In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across |

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		access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high	network facility 206. In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid

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		bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17; FIGS. 6 & 8	collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See also row 20 above*
31. transmitting packet data from one of the plurality of	20(e), 26	Rembrandt does not believe this term requires construction. In the alternative: transmitting packet data [defined above] from one of the multiple sources of packet data [defined above]	transmitting packet data from the only one of the plurality of packet data sources that was allowed by the distributed packet manager to have access to the multiple-access packet channel

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packet data sources having access to the multiple-access packet channel		sources having access to the shared packet channel. Intrinsic Support: FIGS. 3 & 4, element 204; FIGS. 5 & 7; Abstract; "I have realized an alternative approach to the design of TDM-based equipment that supports both synchronous data and packet data and, in addition, provides an efficient substrate for packet handling. In particular, multiple packet data sources share a single TDM channel. As a result, no central packet manager is required to aggregate the packet data. In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data. Each packet application module includes its own TDM bus	Intrinsic Support: FIGS. 4-8C "Before describing it in detail, an overview of this slotted-access method is described. In the slotted-access method, each packet application module, in rotation order, is given an "access window" of time, corresponding to a "bit time-slot" on the TDM bus, to either capture the "multiple-access packet channel" for transmission, or defer and allow the "access window" to advance to the next packet application module in order. Once granted access, that packet application module has sole access to the "multiple-access packet channel" for a period of time, referred to herein as the "access period."" 6:65-7:8. "There is an implied numbering of the packet application modules and "bit time-slots." This implied numbering is hereafter referred to as an "ID number." Generally speaking, a packet application module can attempt to access TDM bus 204-o only when the ID number of the "bit time-slot" matches the ID number of the packet application module." 7:25-31.

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		interface and the network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint. In the receiving direction, each packet application module accepts the entire received packet stream from the network access module and either filters the packets using their address field or transparently forwards the packet data to a packet service." 2:42-65; "An illustrative block diagram of an NAU embodying the principles of this invention is shown in FIG. 3. NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept,	"In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is <u>shared</u> among at least two of the packet application modules. <u>This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module.</u> The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. <u>In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules.</u> (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, <u>this approach makes the entire network bandwidth allocated to packet data</u>

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		multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules." 3:39-61; "In accordance with the principles of the invention, packet/TDM interface 310 synchronizes packet data retrieved from buffer 315 for insertion into an appropriate time slot on TDM bus 204. The latter is shown as actually comprising two TDM buses. TDM bus 204-o is used for "outbound" traffic through NAM 205 to network interface 206. Conversely, TDM bus 204-i is used for "inbound" traffic from the network. Typically, in the art, TDM bus 204-i and 204-o are symmetrical, e.g., if time-slot 0 is used for status and control information on the "inbound" TDM bus, time-slot 0 of the "outbound" TDM is similarly used for status and	dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "As described above, each packet application module must contend for the "multiple-access packet channel." If a packet application module "grabs" the "multiple-access packet channel" that packet application module then transmits using the full 384 Khz of bandwidth." 6:7-10. "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:53-64.

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		control information." 4:25-36; "The "multiple-access packet channel" in this case can be considered a continuous sequence of bits with no framing boundaries other than those of the protocol. As such, the starting point of a packet may lie anywhere in the "multiple-access packet channel." An illustrative sequence of frames is shown in FIG. 5. Frame 1 includes time slots 1 through N, where, as mentioned above, each time-slot represents a 64 Kbit DS0 channel. In this example, it is assumed that N is equal to 64 time-slots. Each frame repeats every 125 micro-seconds and each time-slot is further broken down into a sequence of 8 bits as shown in FIG. 5. Each bit is hereafter referred to as a "bit time-slot." It should be noted that the term "time-slot" refers to a collection of "bit time-slots." Time-slots 1-6 represent the "multiple-access packet channel." As described above, since HDLC is a bit-oriented layer 2 protocol, this allows the packet data to begin and end anywhere in a time-slot. Consequently, each packet is mapped into a plurality of "bit time-slots" within time-slots 1 through 6 on TDM bus 204, rather than the DS0 channels representing each time-slot as a whole. This is illustrated in FIG. 5,	*See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance *See also row 20 above*

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		where packet 50 begins with "bit time-slot" 7 in time-slot 4, of frame 1, and ends with "bit time-slot 3" in time-slot 2 of frame 4. As illustrated by the starting and ending time of packet 50, of FIG. 5, these bit intervals do not have to conform to time slot boundaries into which the packets are mapped and inserted." 5:43-6:5; "Since the TDM bus 204 is full duplex, as represented by separate data highways TDM bus 204-i and TDM bus 204-o, NAU 200 may have an asymmetric access protocol. That is, the access protocol for the inbound direction can be different from the access protocol described below for the outbound direction." 6:36-41; "In accordance with the invention, a Time-division Multiple Access with Collision Avoidance (TDMA/CA) scheme is used for the outbound direction to regulate access to the "multiple-access packet channel." In particular, the synchronous property of TDM bus 204 provides the means to implement a slotted-access method to avoid collisions. This slotted-access method enables each packet application module to contend for the "multiple-access packet channel," and avoid packet	

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		collisions, in a fair and efficient manner. In this embodiment, the slotted-access method is implemented by packet/TDM interface 310 of each packet application module." 6:52-64; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17	
_32._ network access manager/module	8, 26	A device, process or algorithm for controlling the assignment of synchronous and packet data portions on a time division multiplexed bus [defined above], and for passing data between the bus and a network. Intrinsic Support: FIGS. 3, 4, 6 element 205; Prior Art FIGS. 1, 2; "NAU 200 provides access to a T1 facility for frame relay services as well as synchronous data	component of the network access unit that provides the interface between the TDM bus in the network access unit and at least one network facility Intrinsic Support: FIGS. 1-3 "Unfortunately, the instantaneous, or peak, data rate of all outbound packet streams taken together may be greater than the "fixed amount of TDM bandwidth"

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		transport. For simplicity, data endpoints, synchronous or packet, are not shown. NAU 200 includes network access module (NAM) 205, synchronous application modules 220-1 to 220-n, and packet application modules 215-1 to 215-n. NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 205 via TDM bus 204, as is known in the art. In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below)." 3:40-53; "This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module**.** The 'multiple-access packet channel' provides a single channel for communicating all packet data to, or from, NAM 205. In effect, this 'multiple-access packet channel' resembles a packet 'local area network' (LAN) in many respects, except that the bandwidth of the 'multiple-access packet channel' is closely matched (or equal) to that allocated for packet traffic across network facility 206. In this case, each packet application module	allocated for packet data on the network interface." 1:65-2:1. "NAM 205 provides the interface between TDM bus 204 and network facility 206, which is representative of a T1 facility." 3:46-48. "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below) . . . and the packet manager is eliminated . . . ." 3:51-61 "In accordance with the inventive concept, multiple packet application modules now share a single TDM channel (described below). Each of the plurality of packet application modules couple packet data equipment (not shown), e.g., a data terminal, to TDM bus 204, and the packet manager is eliminated. Indeed, the function of the packet manager is now distributed among the various packet application modules that created the need for it in the first place. This distribution of the packet manager is represented by the inclusion of packet managers 216-1 through 216-n in the respective packet application modules. A block diagram of illustrative packet application module 215-n is shown in FIG. 4. Other than the inventive concept, the components of packet

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		must contend for the bandwidth of the 'multiple-access packet channel' with the other packet application modules. (Although, the nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.) NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the 'multiple-access packet channel.'" 4:62-5:20; "A method illustrating this slotted-access technique for use in the packet application module of FIG. 4 is shown in FIG. 8. The steps shown in FIG. 8 have	application module 215-n are well-known and will not be described in detail. Packet application module 215-n includes packet interface processor 305, buffer 315, and packet/TDM interface 310." 3:51-67. "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is <u>shared</u> among at least two of the packet application modules. <u>This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module.</u> The "multiple-access packet channel" provides a single channel for communicating all packet data to, or from, NAM 205." 4:56-64 (emphasis added). "In effect, this "multiple-access packet channel" resembles a packet "local area network" (LAN) in many respects, except that the bandwidth of the "multiple-access packet channel" is closely matched (or equal) to that allocated for packet traffic across network facility 206. <u>In this case, each packet application module must contend for the bandwidth of the "multiple-access packet channel" with the other packet application modules.</u> (Although, the

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		been divided into different 'subroutines' for simplicity, i.e., an 'initialize subroutine'(FIG. 8A), 'request to transmit a packet subroutine' (FIG. 8B), and a 'wait for PHOLD' subroutine (FIG. 8C). In step 505, packet application module 215-n is initialized, e.g., via a power-up sequence, and determines its ID number, e.g., via a hardware strap or software configuration. During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the 'multiple-access packet channel.' Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting 'bit time-slots' of the 'multiple access packet channel' in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each 'bit time-slot' of TDM bus 204-o that is associated with the 'multiple-access packet channel.' The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value." 9:17-38; "NAU 100 includes network access module 115-1	nature of a TDM bus prevents any packet application module from using more bandwidth than is available from the network, this approach makes the entire network bandwidth allocated to packet data dynamically available to each packet application module as a channel for the transport of packet data.)" 4:64-5:10. "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules. The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." 5:11-20. "These properties are only applicable to the outbound (toward the network) direction, where multiple packet sources are contending for a fixed network pipe." 6:33-35

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		105, synchronous application modules 120-1 to 120-n, packet application modules 115-1 to 115-n, and packet manager 110. NAM 105 provides the interface between time-division-multiplexing (TDM) bus 104 and network facility 106, which is representative of a T1 facility. The synchronous application modules couple synchronous data equipment (not shown), e.g., telephone equipment, to NAM 105 via TDM bus 104." 1:30-36.	"During this initialization, NAM 205 of FIG. 3 allocates the time-slots associated with the "multiple-access packet channel." Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted)." 9:25-31. 10/1/97, Reasons for Allowance, "The network access module receives a single, continuously multiplexed, packet stream for transmission to an opposite endpoint." *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance
33. a counter for counting time-slots representing the second portion of the predefined bandwidth	11(d)	Rembrandt does not believe this term requires construction. In the alternative: a device that measures time slots in the second portion of the predefined bandwidth [defined above]. Intrinsic support: FIG. 4, element 310;	a counter that counts only the time slots in the second portion of the predefined bandwidth Intrinsic support: FIGS. 5-8C "In other words, each packet application module only

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		"In an embodiment of the invention, a plurality of packet data sources, e.g., packet application modules, and synchronous data sources, e.g., synchronous application modules, are coupled to the same TDM bus for communicating data to a network access module. In particular, a portion of the TDM bandwidth allocated to packet data is treated as a "multiple-access packet channel." This allows packet application modules on the TDM bus to share, and contend for, the entire TDM bandwidth allocated to packet data." 2:49-57; "In accordance with the invention, a portion of the bandwidth of TDM bus 204 is pre-assigned to all the packet data. In particular, this packet-dedicated portion of the bandwidth is referred to herein as a "multiple-access packet channel," which is shared among at least two of the packet application modules. This is in contrast to allocating a fixed fraction of the TDM bandwidth to each packet application module." 4:56-62; "NAM 205 communicates to all application modules and controls time-slot allocation among the synchronous modules and the packet modules.	counts those "bit time-slots" assigned to the "multiple-access packet channel." 7:35-38. In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the "multiple-access packet channel." The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value." 9:33-38 "Upon receiving the BUFFER NOT EMPTY signal, TDM/packet interface 310 waits for the "access window" in step 525. Once the "access window" matches, i.e., the ID number of packet application module 215-n matches the current value of the counter, i.e., the "bit time-slot" ID number, TDM/packet interface 310 asserts the PREQ signal in step 530." 9:56-62. *See also* '858 patent file history at 4/4/97 Office Action; 8/4/97 Amendment; 10/1/97 Notice of Allowance

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		The control of time-slot allocation can be performed either over TDM bus 204 or another bus (not shown). In this example, it is assumed that a portion of the TDM bus bandwidth is allocated to control and status information, as known in the art. In accordance with the principles of the invention, the time-slots allocated by NAM 205 to the packet application modules are the "multiple-access packet channel." In this example, it is assumed that every time-frame is comprised of a plurality of 64 Kbit (DS0) channels, and it is assumed that the "multiple-access packet channel" is any grouping of these DS0 channels. Although not a requirement, it is also assumed that the "multiple-access packet channel" is composed of a subset of contiguous DS0 channels available on the bus. In this case, this corresponds to time-slots 1, 2, 3, 4, 5, and 6, of every frame. The remaining time-slots are allocated to synchronous data and control/status information. The allocation of the above-mentioned six time-slots yields a "multiple-access packet channel" with a bandwidth of 384 Khz. The number of DS0 channels allocated on the inbound and outbound data highways are assumed to the be same, so that	

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		equal bandwidth is assured in both directions. (As described above, it is assumed that TDM bus 204-i and TDM bus 204-o are symmetrical, i.e., time-slots 1 through 6 are used for the "multiple-access packet channel" for inbound and outbound traffic.) Finally, it is assumed that this 384 Khz bandwidth is equal to the bandwidth allocated over the network facility for the same packet traffic, i.e., NAM 205 is not required to buffer the packet data." 5:11-42; "The properties desired for packet transport on the "multiple-access packet channel" are high bandwidth efficiency and deterministic fairness. Bandwidth efficiency is a measure of how closely the packet utilization oft he available (fixed) TDM bandwidth matches the offered packet load. It also measures efficiency of the channel as the offered packet load exceeds the available bandwidth. Fairness describes how a chosen priority scheme affects the comparative delay of packets through the system under bandwidth contention with multiple packet sources." 6:15-24; "Packet/TDM interface 310 uses the assignment information from NAM 205 as the synchronizing	

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		signal to begin counting "bit time-slots" of the "multiple access packet channel" in step 510 (provided that the PREQ signal is not asserted). In this example, it is assumed that packet/TDM interface 310 includes a counter to count each "bit time-slot" of TDM bus 204-o that is associated with the "multiple-access packet channel." The counter included within packet/TDM interface 310 rims continuously and is controlled by the PREQ signal, i.e., if PREQ is asserted--no counting takes place and the count holds at the last value." 9:28-38; "Also, because the bandwidth of a TDM bus may be divided into many separate logical channels, data with different formats and access methods, such as isochronous and packet data, may be combined in the system. Mother variation is to use the time-slots to control contention access, as opposed to the "bit-time slots," described above." 11:12-17; FIGS. 6 & 8	

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1. the preamble operating to frame the message and to delimit the message from silence	1(b), 12(b), 23(b), 24, 34(b), 35	Rembrandt does not believe this term requires construction. In the alternative: an initial pattern of bits to frame the message and to delimit the message from silence. Intrinsic Support: "A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data. The lower rate symbols of the preamble significantly increase the probability that the decoder will decode the preamble symbols error free. Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel. The first symbol of the preamble can be transmitted at the lower symbol rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission. The end of the communication message can be reliably delimited by sending the first symbol containing only bits from a next cell of information at	the preamble includes a first symbol transmitted at a power level higher than all other preamble symbols to precisely identify the beginning of the message and communication link control information used to precisely identify the end of the message Intrinsic Support: Support for the part of the construction re "communication link control information used to precisely identify the end of the message" FIGS. 3A-6 "Robustly delimiting the beginning of a message enables a receiving transceiver to reliably begin immediately decoding the message at the correct symbol. Likewise, robustly delimiting the end of a message enables a receiving transceiver to reliably decode the entire message through the final symbol and then stopping so as to prevent data loss and to prevent the inclusion of any false data. Furthermore, by communicating the end of message indicator to a receiving transceiver prior to the actual end of the message, line turnaround time (i.e., idle time on the

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		a lower symbol rate and including an extra bit in that symbol. The extra bit can be set to indicate to a receiver whether the last cell of information has just begun." Abstract;	line between transmissions) can be reduced, thereby increasing the effective use of the available line bandwidth." 2:23-34.
			"Thus, it would be desirable to have a robust manner in which to detect the beginning and end of a transmission so that line bandwidth can be most efficiently allocated." 2:51-52.
		Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as "framing" the data to be transmitted. Due to the switched-carrier nature of the transmission, silence precedes this preamble and it is of course important for all symbols in this preamble to be received error free. It is also desirable to have the ability to precisely delimit the beginning and end of a transmission to within one transmitted symbol interval. Robustly delimiting the beginning of a message enables a receiving transceiver to reliably begin immediately decoding the message at the correct symbol. Likewise, robustly delimiting the end of a message enables a receiving transceiver to reliably decode the entire message through the final symbol and then stopping so as to prevent data loss and to prevent the inclusion of any false data." 2:13-29	"The present invention provides an improved system and method for robustly delimiting a message transmission in switched-carrier communication systems. The invention provides a method and system for transmission of a message preamble in which transmission of the preamble is more robust than the data. In this manner, the beginning and end of a transmission can be robustly delimited and channel control information can be reliably conveyed to a receiving transceiver." 2:59-67.
			"For example, if the normal data rate is five (5) bits per symbol, then a symbol rate of two (2) bits per symbol has a significantly (approximately 9 dB) higher noise margin than the five (5) bit per symbol data rate, thereby allowing the symbols that are encoded at the lower rate of two (2) bits per symbol

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		"Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel." 3:5-12; "The present invention can also be viewed as a method for robust transmission delimiting comprising the steps of applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information, and encoding the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel." 3:22-30.	to be very robustly and reliably decoded by a receiving device. In this manner, the preamble 40, which is sent at the beginning of every communication message 31, can be made sufficiently robust so that the chance that it will always be received error free is greatly increased. Although very robust, there are still situations in which the symbols into which the preamble bits are encoded can be corrupted." 7:31-42. "The format bits 66 indicate whether the optional administrative header 42 is being sent, whether one or more ATM cells are being sent, or whether both or neither are being sent. As described previously, the receiver uses this information in conjunction with the transmit rate from bits 62 to identify the special symbols at the start of each ATM cell and to determine the symbol that is the last in the message." 11:15-22 (emphasis added). "For efficient operation, it is desirable that the beginning and end of each transmission be robustly and precisely identified (to within one (1) symbol interval). The beginning and end of each transmission are preceded and followed by silence on the line." 11:59-63.

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			"For example, the robust preamble and transmission delimiting system and method are applicable to all switched-carrier transmission methodologies in which it is desirable to reliably convey channel establishment information and reliably delimit the beginning and end of each communication message." 18:6-14. "The basic function provided by framing in TDD transmission of ATM cells is to mark the beginning and end of the transmission." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 3. "Reliable detection of the beginning and ending symbols is essential for efficient usage of the line bandwidth so it is beneficial if the framing technique can be made more robust than the data encoding (i.e. errors will occur in the data frame before line usage discipline breaks down due to failure to properly detect transmission boundaries). Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 4. "The end-of-frame symbol is received at least 35

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			symbols (at a maximum rate of 12bps) before the actual end of frame occurs." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 8. "Framing (i.e. delimiting) of transmission." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 1. "Indicating End of Message As mentioned above, if the transmit data rate is known, with ATM payload data, the symbols that are candidates to be the last symbol are both exactly known and sufficiently infrequent that . . ." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 5. "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as "framing" the data to be transmitted. Due to the switched-carrier nature of the

U.S. Patent No. 6,950,444 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			transmission, silence precedes this preamble and it is of course important for all symbols in this preamble to be received error free. It is also desirable to have the ability to precisely delimit the beginning and end of a transmission to within one transmitted symbol interval." 2:13-22. Support for the part of the construction dealing with "first symbol transmitted at a power level higher than all other preamble symbols" "A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data" Abstract "The first symbol of the preamble can be transmitted at the lower symbol rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission." Abstract. "The present invention relates generally to communications systems, and more particularly, to a system and method for a robust preamble and

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			transmission delimiting in a switched-carrier transceiver." 1:19-22. "Due to the switched-carrier nature of the transmission, silence precedes this preamble and it is of course important for all symbols in this preamble to be received error free." 2:18-19. "To improve message delimiting, existing techniques use special marker symbols whose symbol indices are greater than those used to encode data. At N bits per symbol (bps) data is encoded using symbol indices 0 through $2.\text{sup}.N - 1$. The special symbols use indices $2.\text{sup}.N$ and above. While these special marker symbols are useful for marking the beginning and end of a transmission, their placement at the outer edges of a constellation raises the peak signal, thus increasing the peak to average ratio (PAR) across all data rates by as much as 4 dB. Unfortunately, discrimination of special symbols has the same error threshold as does decoding of data. Thus, it would be desirable to have a robust manner in which to detect the beginning and end of a transmission so that line bandwidth can be most efficiently allocated. Furthermore, it would be desirable to robustly transmit a message preamble

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			including control information thereby greatly improving the probability that the preamble is received error free." 2:39-56. "In accordance with another aspect of the invention, the first symbol 55 representing the first bits in the preamble 40 can be sent using an increased power level, thereby clearly and robustly delimiting the beginning of the communication message 31. The effect of this increased power level symbol 55 will be explained in greater detail below with respect to FIGS. 4A and 4B." 7:49-55. "In accordance with another aspect of the invention, the first symbol 55 is encoded at a rate of two (2) bits per symbol and has its energy increased to a point at which noise on the communication channel is unlikely to cause a receiver to erroneously interpret the first symbol 55 as silence. Likewise the increased energy makes it unlikely that noise on the communication channel will cause the receiver to erroneously interpret an interval of the silence that precedes each message as the starting symbol of a message. It has been found that an energy increase of 3dB is sufficient. This aspect of the invention will be described in greater detail below with respect to

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			FIGS. 4A and 4B. In this manner, the beginning of each transmission can be clearly and robustly delimited. The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded at two (2) bits per symbol, but do not have their energy increased." 10:15-31. "In accordance with an aspect of the invention, the first symbol (symbol 55 of FIG. 3B) in the preamble 40 is transmitted with increased energy, thereby increasing the probability that it will be reliably detected by the decoder of the receiving device. In this manner, the beginning of each transmission is clearly and robustly delimited. The signal point "b" in FIG. 4A is an exemplar one of four (4) two (2) bit per symbol constellation points that are transmitted at an increased energy level." 12:6-14. "Accordingly, by boosting the energy of the first symbol (symbol 55 of FIG. 3B) transmitted in a communication message (31 of FIG. 3A), there is a significantly higher probability that the boosted symbol will be reliably decoded and not be mistaken for silence. Nor will silence be mistaken for this boosted energy first symbol." 12:20-26.

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			"In accordance with another aspect of the invention, the four constellation points labeled "b" in FIG. 4B represent the first symbol (symbol 55 of FIGS. 3A and 3B), which energy is boosted by 3 dB." 12:45-48. "In this manner, the boosted symbol represented by constellation points "b" can be used to reliably indicate the start of a message without requiring a higher transmit level capability than that needed for normal data transmission. The non-boosted two (2) bit per symbol constellation points indicated as "c" (having a significantly higher signal-to-noise ratio than that of the normal five (5) bit per symbol data) are used to transmit all symbols of the preamble after the first symbol." 12:59-67. "Some intervals of silence necessarily occur between transmissions because the transition from silence to the first symbol of the preamble is the manner in which the beginning of the next transmission is delimited." 14:2-6. "The first symbol is forwarded via connection 301 to gain reduction element 302. Gain reduction element 302 reduces the gain of the first symbol and supplies that reduced energy symbol via connection 304 to

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			multiplexer 306." 16:35-38. "Adding the boost is essential to provide a robust indication of the start of the message when operating at the worst case signal-to-noise conditions. … Noise peaks on silence could frequently be mistaken for the first symbol and noise peaks on the first symbol may frequently result in it being classified as silence. By boosting the amplitude of the symbols in the PMD preamble by 3 dB, the threshold to discriminate the starting symbol can be set well above the maximum expected excursion of silence plus noise and the likelihood of starting symbol being corrupted so much that it falls under this threshold is significantly reduced." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. FIGS. 2B-6; Provisional Applications *See also* '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment

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2. a plurality of bits representing communication link control information	1(b), 12(b), 23(b), 24, 34(b), 35	Rembrandt does not believe this term requires construction. In the alternative: multiple bits used to convey communication link control information [defined above]. Intrinsic Support: "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as 'framing' the data to be transmitted." 2:13-17; "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL	transmit rate bits, maximum receive rate bits, address bits (where there is more than one remote), and message format bits, decoded by the receiver to control communications over the link Intrinsic Support: Figs. 2B, 3B; 7, 8, 9 (elements 317, 319, 322 and 326) "Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel." Abstract. "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver." 2:13-15. "Furthermore, it would be desirable to robustly transmit a message preamble including control information thereby greatly improving the probability that the preamble is received error free." 2:53-56. "The invention provides a method and system for

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		transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether ATM cells follow the preamble, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates." 9:35-55; '444 Patent File History, Paper 8, pg. 2.	transmission of a message preamble in which transmission of the preamble is more robust than the data. In this manner, the beginning and end of a transmission can be robustly delimited and channel control information can be reliably conveyed to a receiving transceiver." 2:61-67. "Communication message 31 begins with preamble 40 followed by optional administrative header 42. In accordance with an aspect of the invention, all communication messages, regardless of the content, begin with preamble 40. Administrative header 42 is optional and can be used to send information that is neither part of the preamble 40 or of any data to follow." 6:33-35. "For example, the administrative header 42 could convey a description of noise level conditions at one end so the other end may opt to increase or reduce the power level of its transmission as necessary. Likewise, the administrative header 42 sent by a remote transceiver could contain information regarding the amount of payload information that the remote transceiver is ready to transmit and its relative priorities so that the control transceiver could alter the amount of time that this remote transceiver is

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			given to transmit its data (relative to any other transceivers connected to the line). When the payload data comprises ATM cells, the control transceiver could use messages conveyed by the administrative header 42 to direct remote devices to activate or deactivate various ATM virtual circuits." 6:35-49. "If data is included in communication message 31, one or more ATM cells follow the optional administrative header 42." 6:50-51. "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols." 7:16-17. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL

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			transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether ATM cells follow the preamble, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates." 9:35-55. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits." 10:32-35. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the maximum receive rate at which the transmitting device can receive." 10:57-59. "Inherently included in these receive rate bits 63 are

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			commands that instruct the opposite device to either increase or decrease its transmit rate." 10:60-62. "In accordance with an aspect of the invention, the address bits 64 need only be used when the control DSL transceiver 100 is communicating with a plurality of remote DSL transceivers in what is commonly referred to as "multi-point" mode." 10:66-11:3. "The format bits 66 indicate whether the optional administrative header 42 is being sent, whether one or more ATM cells are being sent, or whether both or neither are being sent. As described previously, the receiver uses this information in conjunction with the transmit rate from bits 62 to identify the special symbols at the start of each ATM cell and to determine the symbol that is the last in the message. Robust transmission of this information at the start of each message allows the transmitter to dynamically modify the message format as needed from one message to the next." 11:16-22. "The beginning and end of each transmission are preceded and followed by silence on the line." 11:61-63.

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			"If there are multiple remote DSL transceivers 150 and 155, then the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the remote address from remote address element 202, which bits are then forwarded via connection 209 to multiplexer 214." 15:30-35. "The following preamble symbols are all forwarded via connection 301 directly to multiplexer 306, which forwards these symbols via connection 307 for decoding by two (2) bit per symbol preamble decoder 308. The decoded bits are forwarded via connection 309 to preamble descrambler 311 as mentioned above. These bits are then forwarded in order via connections 324, 321, 318 and 316 to transmit rate element 326, receive rate element 322, remote address element 319 and message format element 317, respectively. … As shown, the value of N, which is the bits per symbol value used for the N bits per symbol, or N-1 bits per symbol decoding is controlled by the just received transmit rate bits that have been stored in transmit rate element 326." 16:50-17:8. "At the appropriate time, receive sequencer 328

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			commands the multiplexer 342 via connection 347 to forward the bits via connection 344 to payload descrambler 336. … Receive sequencer 328 determines the presence or absence of the administrative header and ATM cells via the just received message format bits that have been stored in element 317 and provided to receive sequencer 328 via connection 327." 17:9-29. "This is a technique for robust framing of a block of Asynchronous Transfer Mode (ATM) cells and encoding of other critical link control signals." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1 "The existing version of MVL attaches a TC (transmission convergence) layer header to each message. Among the functions of this header are to identify the tributary to which the message is addressed, indicate if the tributary is expected to respond (polling) and indicate that a special non-data ("administrative") message follows." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 4.

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			"In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The final symbol, used only in multipoint modes, is either the address of the tributary station that is to transmit next (if sent by the ATU-C) or the address of the responding tributary station (if sent by the ATU-R)." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1 "The signals that communicate changes in transmitted data rate, request for a change in received data rate (up, down, no change, minimum rate or retrain) and for multipoint, the address of the polled tributary, are also sent with at least 3dB of additional noise margin. . . . The TC layer header is sent only when needed for some administrative functions." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S.

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			Provisional Application No. 60/150,436 at 8 "Therefore, it seems reasonable to require that the signals carrying information needed to manage usage of an MVL circuit have more robustness in terms of susceptibility to line errors than those that simply carry payload data. These critical functions are considered to be the following: Framing (i.e. delimiting) of transmissions Auto-rating, both to indicate the rate used for transmission and to request changes in the data rate of received data Address of the ATU-R from whom a response is expected (i.e. polled address). Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 1. "Control data: Data, which is transmitted during the control or header segment of each frame and used to control modem operation. The control data is independent of the user data." Paradyne Pinnacle Technology Program, "MVL Modem Line Signaling Procedures and Mechanisms", *submitted with* U.S. Provisional Application No. 60/150,436, at 4.

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			See also '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment

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3. communication link control information	1(b), 12(b), 23(b), 24, 34(b), 35	A programmable pattern of bits to convey information regarding the communication. Intrinsic Support: "A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data. The lower rate symbols of the preamble significantly increase the probability that the decoder will decode the preamble symbols error free. Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel. The first symbol of the preamble can be transmitted at the lower symbol rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission. The end of the communication message can be reliably delimited by sending the first symbol containing only bits from a next cell of information at a lower symbol rate and including an extra bit in that symbol. The extra bit can be set to indicate to a receiver whether the last cell of information has just	transmit rate bits, maximum receive rate bits, address bits (where there is more than one remote), and message format bits, decoded by the receiver to control communications over the link Intrinsic Support: Figs. 2B, 3B; 7, 8, 9 (elements 317, 319, 322 and 326) "Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel." Abstract. "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver." 2:13-15. "Furthermore, it would be desirable to robustly transmit a message preamble including control information thereby greatly improving the probability that the preamble is received error free." 2:53-56. "The invention provides a method and system for

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		begun." Abstract; "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver." 2:13-17; "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether ATM	transmission of a message preamble in which transmission of the preamble is more robust than the data. In this manner, the beginning and end of a transmission can be robustly delimited and channel control information can be reliably conveyed to a receiving transceiver." 2:61-67. "Communication message 31 begins with preamble 40 followed by optional administrative header 42. In accordance with an aspect of the invention, all communication messages, regardless of the content, begin with preamble 40. Administrative header 42 is optional and can be used to send information that is neither part of the preamble 40 or of any data to follow." 6:33-35. "For example, the administrative header 42 could convey a description of noise level conditions at one end so the other end may opt to increase or reduce the power level of its transmission as necessary. Likewise, the administrative header 42 sent by a remote transceiver could contain information regarding the amount of payload information that the remote transceiver is ready to transmit and its relative priorities so that the control transceiver could alter the amount of time that this remote transceiver is

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		cells follow the preamble, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates." 9:35-55; '444 Patent File History, Paper 8, pg. 2.	given to transmit its data (relative to any other transceivers connected to the line). When the payload data comprises ATM cells, the control transceiver could use messages conveyed by the administrative header 42 to direct remote devices to activate or deactivate various ATM virtual circuits." 6:35-49. "If data is included in communication message 31, one or more ATM cells follow the optional administrative header 42." 6:50-51. "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols." 7:16-17. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL

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			transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether ATM cells follow the preamble, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates." 9:35-55. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits." 10:32-35. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the maximum receive rate at which the transmitting device can receive." 10:57-59. "Inherently included in these receive rate bits 63 are

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			commands that instruct the opposite device to either increase or decrease its transmit rate." 10:60-62. "In accordance with an aspect of the invention, the address bits 64 need only be used when the control DSL transceiver 100 is communicating with a plurality of remote DSL transceivers in what is commonly referred to as "multi-point" mode." 10:66-11:3. "The format bits 66 indicate whether the optional administrative header 42 is being sent, whether one or more ATM cells are being sent, or whether both or neither are being sent. As described previously, the receiver uses this information in conjunction with the transmit rate from bits 62 to identify the special symbols at the start of each ATM cell and to determine the symbol that is the last in the message. Robust transmission of this information at the start of each message allows the transmitter to dynamically modify the message format as needed from one message to the next." 11:16-22. "The beginning and end of each transmission are preceded and followed by silence on the line." 11:61-63.

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			"If there are multiple remote DSL transceivers 150 and 155, then the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the remote address from remote address element 202, which bits are then forwarded via connection 209 to multiplexer 214." 15:30-35. "The following preamble symbols are all forwarded via connection 301 directly to multiplexer 306, which forwards these symbols via connection 307 for decoding by two (2) bit per symbol preamble decoder 308. The decoded bits are forwarded via connection 309 to preamble descrambler 311 as mentioned above. These bits are then forwarded in order via connections 324, 321, 318 and 316 to transmit rate element 326, receive rate element 322, remote address element 319 and message format element 317, respectively. … As shown, the value of N, which is the bits per symbol value used for the N bits per symbol, or N-1 bits per symbol decoding is controlled by the just received transmit rate bits that have been stored in transmit rate element 326." 16:50-17:8. "At the appropriate time, receive sequencer 328

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			commands the multiplexer 342 via connection 347 to forward the bits via connection 344 to payload descrambler 336. … Receive sequencer 328 determines the presence or absence of the administrative header and ATM cells via the just received message format bits that have been stored in element 317 and provided to receive sequencer 328 via connection 327." 17:9-29. "This is a technique for robust framing of a block of Asynchronous Transfer Mode (ATM) cells and encoding of other critical link control signals." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1 "The existing version of MVL attaches a TC (transmission convergence) layer header to each message. Among the functions of this header are to identify the tributary to which the message is addressed, indicate if the tributary is expected to respond (polling) and indicate that a special non-data ("administrative") message follows." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 4.

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			"In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The final symbol, used only in multipoint modes, is either the address of the tributary station that is to transmit next (if sent by the ATU-C) or the address of the responding tributary station (if sent by the ATU-R)." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1 "The signals that communicate changes in transmitted data rate, request for a change in received data rate (up, down, no change, minimum rate or retrain) and for multipoint, the address of the polled tributary, are also sent with at least 3dB of additional noise margin. . . . The TC layer header is sent only when needed for some administrative functions." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S.

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			Provisional Application No. 60/150,436 at 8 "Therefore, it seems reasonable to require that the <u>signals carrying information needed to manage usage of an MVL circuit</u> have more robustness in terms of susceptibility to line errors than those that simply carry payload data. These <u>critical functions</u> are considered to be the following: Framing (i.e. delimiting) of transmissions Auto-rating, both to indicate the rate used for transmission and to request changes in the data rate of received data Address of the ATU-R from whom a response is expected (i.e. polled address). Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 1. "Control data: Data, which is transmitted during the control or header segment of each frame and used to control modem operation. The control data is independent of the user data." Paradyne Pinnacle Technology Program, "MVL Modem Line Signaling Procedures and Mechanisms", *submitted with* U.S. Provisional Application No. 60/150,436, at 4.

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			See also '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment
<u>4.</u> means for applying a preamble to a communication message…the preamble including a plurality of bits representing communication link control information	23(b), 24	<u>Means plus function term</u>: "means for applying a preamble to a communication message". <u>Function</u>: Applying a preamble to a communication message. <u>Structure</u>: A sequencer and multiplexer, or the equivalents. FIG. 8 (elements 224 and 236). <u>Intrinsic Support:</u> FIG. 8, elements 224 and 236; "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a	Means plus function element to be construed pursuant to 112, ¶ 6. <u>Function</u> – applying a preamble to a communication message, the preamble operating to frame the message and delimit the message from silence, the preamble including a plurality of bits representing communication link control information (*See rows 1 & 2 above* for construction of limitations of this function) <u>Structure</u> – includes transmit sequencer **236**, message format **201**, the remote address **202**, the receiving rate **204** and the transmission rate **205**, along with the multiplexer **214**. **201-202** and **204, 206** are computer readable memory that separately store bits representing the communication link control information (*see* claim 1(b)) and separately supply those bits to the multiplexer **214** when commanded to

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		plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel." 3:5-12; "The present invention can also be viewed as a method for robust transmission delimiting comprising the steps of applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information, and encoding the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel." 3:22-30; "Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as "framing" the data to be transmitted." 2:13-17. "Robustly delimiting the beginning of a message enables a receiving transceiver to reliably begin immediately decoding the message at the correct	do so by the multiplexer <u>Intrinsic Support:</u> *See rows 1 & 2 above* FIGS. 3B; 7-9 "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 36 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. . . . The next two (2) bits of the transmit rate (62 of FIG 3. B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 11. . . transmit sequencer commands the multiplexer 214 via connection 242 to select the two (2) bits representing the remote address from remote address element 202, which bits are then forwarded via connection 209 to multiplexer 214. . . Transmit sequencer 236 senses if

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		symbol. Likewise, robustly delimiting the end of a message enables a receiving transceiver to reliably decode the entire message through the final symbol and then stopping so as to prevent data loss and to prevent the inclusion of any false data." 2:23-29; "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117. The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four	an administrative header 42 and/or ATM cells 44, 45, 46 are available for transmission via connections 232 and 234, respectively, and uses this information to prepare the message format indicator which is loaded by the transmit sequencer 236 via connection 207. the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (20 bits representing the message format from element 201, which bits are then forwarded via connection 208 to multiplexer 214 . . . . The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117." 15:3-57. *See also* '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment

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		(4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols, are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117." 15:3-28.	
5. an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a	1(c)	Rembrandt does not believe this term requires construction. In the alternative: a mechanism adapted to convert preamble bits into multiple symbols, where the symbols are encoded using a lower bit to symbol rate than the maximum rate capable of being supported over a communication channel [defined above]. Intrinsic Support: "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of	an encoder converts the preamble bits into symbols at a lower bit per symbol rate than the maximum receive rate specified in the preamble that was just received Intrinsic Support: FIG 3B; 7-9. "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an

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communication channel		FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117. The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols, are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator	encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel." 3:5-12. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) **used to encode data following preamble** 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information **regarding the rate (also in bits per symbol) that the receiver is capable of receiving**, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow." 9:35-48 (emphasis added). "In accordance with an aspect of the invention, all of the symbols in preamble, 40 are encoded at a low bit

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		117." 15:3-28; "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol." 7:15-23.	per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on the communication channel." 9:60-67. "The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded at two (2) bits per symbol, but do not have their energy increased." 10:28-31. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications

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			system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is sent only when it is changed." 10:32-56. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the **maximum receive rate** at which the transmitting device can receive. Inherently included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver

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			to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line." 10:57-65 "In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The first indicates whether an increase or decrease (or no change) is requested in the next transmission sent to the currently transmitting station." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1. "Among the uses of administrative messages are for the ATU-C to direct the ATU-R to use a different data rate in its subsequent transmissions or to inform the ATU-R that the ATU-C will use a different rate on its own subsequent transmission. … One

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			disadvantage of this approach is that corruption of messages containing autorating directives may result in control and tributary stations losing track of the rate at which received messages are encoded." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at4. "The subject invention suggests encoding the rate of every transmission in two symbols encoded at 2 bits per symbol at the beginning of each transmission." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "The rate symbols are followed by one or two more symbols also encoded at 2 bits per symbol. The first of these is always transmitted and indicates what change, if any is requested in the data rate of subsequent transmissions sent to the sending station. The choices could be up one rate, down one rate, no change (as with the existing MVL) with the possible addition of a request for minimum rate or possibly some other indication such as a request for a retrain." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No.

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			60/150,436 at 5. "Next the sequencer configures multiplexer A to select the two bits representing the requested receive rate (or retrain request) which are scrambled and encoded the same way and sent to the modulator via multiplexer C." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 7. "The signals that communicate changes in transmitted data rate, request for a change in received data rate (up, down, no change, minimum rate or retrain) and, for multipoint, the address of the polled tributary, are also sent with at least 3 dB of additional noise margin." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 8. "Robust communication of the transmit rate and the **optional maximum receive rate** in addition to elimination of unnecessary TC layer information contribute to efficient operation of the line." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at

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			3. "Any station can indicate the <u>maximum rate at which it is able to receive data</u> in any transmission by starting the transmit rate field of the PMD header with the escape symbol. This is then followed by two symbols to encode the transmit rate of payload data following the header and then by a second pair of symbols<u> to encode the maximum rate at which this station is able to receive data. Since sending this information lengthen the header by 3 symbols the maximum receive rate indication is typically sent only when a station determines that the station to which it is now transmitting needs to update the maximum transmit rate value it is currently using.</u> … Since outbound transmission typically contain ATM cells for more than one tributary, the ATU-C will normally use the lowest maximum receive rate indicated by all ATU-Rs" Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 4. "The first transmission by the ATU-C to each ATU-R following training would normally include the maximum receiver rate field." Broadband Tech Note

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			313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 6. "The signals that communicate changes in transmitted data rate, maximum received data rate, and the address of the polled tributary are also sent with at least 3 dB of additional noise margin." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 7. *See also* '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment

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6. encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel	12(c), 34(c), 35	Rembrandt does not believe this term requires construction. In the alternative: converting the preamble bits into multiple symbols, where the symbols are encoded using a bit-to-symbol rate that is less than the maximum rate capable of being transmitted over a communication channel [defined above]. Intrinsic Support: "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117.	an encoder converts the preamble bits into symbols at a lower bit per symbol rate than the maximum receive rate specified in the preamble that was just received Intrinsic Support: FIG 3B; 7-9. "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel." 3:5-12. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) **used to encode data following preamble** 40 (the data comprising the optional

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		The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols, are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117." 15:3-28. "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be	administrative header and optional ATM cells), four (4) bits 63 that include information **regarding the rate (also in bits per symbol) that the receiver is capable of receiving,** two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow." 9:35-48 (emphasis added). "In accordance with an aspect of the invention, all of the symbols in preamble, 40 are encoded at a low bit per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on the communication channel." 9:60-67. "The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded

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		transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol." 7:15-30.	at two (2) bits per symbol, but do not have their energy increased." 10:28-31. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to

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			potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is sent only when it is changed." 10:32-56. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the **maximum receive rate** at which the transmitting device can receive. Inherently included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line." 10:57-65 "In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the

U.S. Patent No. 6,950,444	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The first indicates whether an increase or decrease (or no change) is requested in the next transmission sent to the currently transmitting station." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1. "Among the uses of administrative messages are for the ATU-C to direct the ATU-R to use a different data rate in its subsequent transmissions or to inform the ATU-R that the ATU-C will use a different rate on its own subsequent transmission. … One disadvantage of this approach is that corruption of messages containing autorating directives may result in control and tributary stations losing track of the rate at which received messages are encoded." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 4. "The subject invention suggests encoding the rate of every transmission in two symbols encoded at 2 bits per symbol at the beginning of each transmission." Paradyne Patent Disclosure Form 799-0059-2

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "The rate symbols are followed by one or two more symbols also encoded at 2 bits per symbol. The first of these is always transmitted and indicates what change, if any is requested in the data rate of subsequent transmissions sent to the sending station. The choices could be up one rate, down one rate, no change (as with the existing MVL) with the possible addition of a request for minimum rate or possibly some other indication such as a request for a retrain." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "Next the sequencer configures multiplexer A to select the two bits representing the requested receive rate (or retrain request) which are scrambled and encoded the same way and sent to the modulator via multiplexer C." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 7. "The signals that communicate changes in transmitted data rate, request for a change in received

U.S. Patent No. 6,950,444	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			data rate (up, down, no change, minimum rate or retrain) and, for multipoint, the address of the polled tributary, are also sent with at least 3 dB of additional noise margin." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 8. "Robust communication of the transmit rate and the **optional maximum receive rate** in addition to elimination of unnecessary TC layer information contribute to efficient operation of the line." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 3. "Any station can indicate the <u>maximum rate at which it is able to receive data</u> in any transmission by starting the transmit rate field of the PMD header with the escape symbol. This is then followed by two symbols to encode the transmit rate of payload data following the header and then by a second pair of symbols <u>to encode the maximum rate at which this station is able to receive data. Since sending this information lengthen the header by 3 symbols the maximum receive rate indication is typically sent</u>

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			only when a station determines that the station to which it is now transmitting needs to update the maximum transmit rate value it is currently using. … Since outbound transmission typically contain ATM cells for more than one tributary, the ATU-C will normally use the lowest maximum receive rate indicated by all ATU-Rs" Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 4. "The first transmission by the ATU-C to each ATU-R following training would normally include the maximum receiver rate field." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 6. "The signals that communicate changes in transmitted data rate, maximum received data rate, and the address of the polled tributary are also sent with at least 3 dB of additional noise margin." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 7.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			See also '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment

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7. the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel	12(c), 34(c), 35	Rembrandt does not believe this term requires construction. In the alternative: converting the preamble bits into multiple symbols, where the symbols are encoded using a bit-to-symbol rate that is less than the maximum rate capable of being transmitted over a communication channel [defined above]. Intrinsic Support" FIG. 8, element 219; "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to	an encoder converts the preamble bits into symbols at a lower bit per symbol rate than the maximum receive rate specified in the preamble that was just received Intrinsic Support: FIG 3B; 7-9. "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel." 3:5-12. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) **used to encode data following preamble** 40 (the data comprising the optional

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		modulator 117. The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols, are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117." 15:3-28. "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar	administrative header and optional ATM cells), four (4) bits 63 that include information **regarding the rate (also in bits per symbol) that the receiver is capable of receiving**, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow." 9:35-48 (emphasis added). "In accordance with an aspect of the invention, all of the symbols in preamble, 40 are encoded at a low bit per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on the communication channel." 9:60-67. "The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded

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		one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol." 7:15-23.	at two (2) bits per symbol, but do not have their energy increased." 10:28-31. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is sent only when it is changed." 10:32-56. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the **maximum receive rate** at which the transmitting device can receive. Inherently included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line." 10:57-65 "In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The first indicates whether an increase or decrease (or no change) is requested in the next transmission sent to the currently transmitting station." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1. "Among the uses of administrative messages are for the ATU-C to direct the ATU-R to use a different data rate in its subsequent transmissions or to inform the ATU-R that the ATU-C will use a different rate on its own subsequent transmission. … One disadvantage of this approach is that corruption of messages containing autorating directives may result in control and tributary stations losing track of the rate at which received messages are encoded." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 4. "The subject invention suggests encoding the rate of every transmission in two symbols encoded at 2 bits per symbol at the beginning of each transmission." Paradyne Patent Disclosure Form 799-0059-2

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "The rate symbols are followed by one or two more symbols also encoded at 2 bits per symbol. The first of these is always transmitted and indicates what change, if any is requested in the data rate of subsequent transmissions sent to the sending station. The choices could be up one rate, down one rate, no change (as with the existing MVL) with the possible addition of a request for minimum rate or possibly some other indication such as a request for a retrain." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "Next the sequencer configures multiplexer A to select the two bits representing the requested receive rate (or retrain request) which are scrambled and encoded the same way and sent to the modulator via multiplexer C." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 7. "The signals that communicate changes in transmitted data rate, request for a change in received

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			data rate (up, down, no change, minimum rate or retrain) and, for multipoint, the address of the polled tributary, are also sent with at least 3 dB of additional noise margin." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 8. "Robust communication of the transmit rate and the **optional maximum receive rate** in addition to elimination of unnecessary TC layer information contribute to efficient operation of the line." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 3. "Any station can indicate the maximum rate at which it is able to receive data in any transmission by starting the transmit rate field of the PMD header with the escape symbol. This is then followed by two symbols to encode the transmit rate of payload data following the header and then by a second pair of symbols to encode the maximum rate at which this station is able to receive data. Since sending this information lengthen the header by 3 symbols the maximum receive rate indication is typically sent

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			only when a station determines that the station to which it is now transmitting needs to update the maximum transmit rate value it is currently using. … Since outbound transmission typically contain ATM cells for more than one tributary, the ATU-C will normally use the lowest maximum receive rate indicated by all ATU-Rs" Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 4. "The first transmission by the ATU-C to each ATU-R following training would normally include the maximum receiver rate field." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 6. "The signals that communicate changes in transmitted data rate, maximum received data rate, and the address of the polled tributary are also sent with at least 3 dB of additional noise margin." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 7.

U.S. Patent No. 6,950,444	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		CONSTRUCTION AND INTRINSIC EVIDENCE	CONSTRUCTION AND INTRINSIC EVIDENCE
			See also '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment
8. maximum rate capable of being transmitted over a communication channel/ maximum rate capable of being supported over a communication channel	1, 12, 23, 24, 34, 35	The highest bit per symbol rate at which the data portion of the message is sent. Intrinsic Support: "A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data. The lower rate symbols of the preamble significantly increase the probability that the decoder will decode the preamble symbols error free. Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel. The first symbol of the preamble can be transmitted at the lower symbol	an encoder converts the preamble bits into symbols at a lower bit per symbol rate than the maximum receive rate specified in the preamble that was just received Intrinsic Support: FIG 3B; 7-9. "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a

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		rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission. The end of the communication message can be reliably delimited by sending the first symbol containing only bits from a next cell of information at a lower symbol rate and including an extra bit in that symbol. The extra bit can be set to indicate to a receiver whether the last cell of information has just begun." Abstract; "In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol. However, any number of bits per symbol lower than that of the normally transmitted data rate can be used so long as the symbol rate allows a receiving device to more reliably decode those symbols. For example, if the normal data rate is five (5) bits per symbol, then a symbol rate of two (2) bits per symbol has a significantly (approximately 9 dB) higher noise margin than the five (5) bit per	communication channel." 3:5-12. "FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) **used to encode data following preamble** 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information **regarding the rate (also in bits per symbol) that the receiver is capable of receiving,** two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow." 9:35-48 (emphasis added). "In accordance with an aspect of the invention, all of the symbols in preamble, 40 are encoded at a low bit per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate

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		symbol data rate, thereby allowing the symbols that are encoded at the lower rate of two (2) bits per symbol to be very robustly and reliably decoded by a receiving device. In this manner, the preamble 40, which is sent at the beginning of every communication message 31, can be made sufficiently robust so that the chance that it will always be received error free is greatly increased. Although very robust, there are still situations in which the symbols into which the preamble bits are encoded can be corrupted. However, in accordance with another aspect of the invention, because the preamble 40 is sent at the beginning of every communication message 31, even if the preamble 40 is corrupted, only data following that preamble may be affected, i.e., lost due to corruption, if certain bits of the preamble are corrupted." 7:20-48; "Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the	ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on the communication channel." 9:60-67. "The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded at two (2) bits per symbol, but do not have their energy increased." 10:28-31. "The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		maximum rate capable of being supported over a communication channel." 3:5-12; "The present invention can also be viewed as a method for robust transmission delimiting comprising the steps of applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information, and encoding the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel." 3**:**22-30; "Communication channel 16 can be any physical medium over which communications signals can be exchanged, and in the preferred embodiment, is the copper wire pair that extends from a telephone company central office to an end-user location, such as a home or office. Central office 12 includes DSL transceiver 100 connected to communication channel 16. DSL transceiver 100 processes data via connection 14. DSL transceiver 100 exchanges data via connection 14 with any data terminal equipment (DTE), such as a computer or data terminal.." 5:17-28;	condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is sent only when it is changed." 10:32-56. "The receive rate bits 63 allow the transmitting device to communicate to the receiving device the **maximum receive rate** at which the transmitting device can receive. Inherently included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line." 10:57-65

U.S. Patent No. 6,950,444 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
		'444 Patent File History, Paper 8, pg. 2.	"In addition, using this technique, the PMD-layer header is expanded from the single symbol currently used to 3, 4 or 5 symbols. <u>Using this expanded header, the rate at which the transmission is encoded (in bits per symbol) is conveyed independently for each transmission</u>. Two symbols encoded at 2 bits per symbol are transmitted at the beginning of the block of cells to convey the rate at which the following data (in this same transmission) has been encoded. … The first indicates whether an increase or decrease (or no change) is requested in the next transmission sent to the currently transmitting station." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 1. "Among the uses of administrative messages are for the ATU-C to direct the ATU-R to use a different data rate in its subsequent transmissions or to inform the ATU-R that the ATU-C will use a different rate on its own subsequent transmission. … One disadvantage of this approach is that corruption of messages containing autorating directives may result in control and tributary stations losing track of the rate at which received messages are encoded."

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			Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at4. "The subject invention suggests encoding the rate of every transmission in two symbols encoded at 2 bits per symbol at the beginning of each transmission." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "The rate symbols are followed by one or two more symbols also encoded at 2 bits per symbol. The first of these is always transmitted and indicates what change, if any is requested in the data rate of subsequent transmissions sent to the sending station. The choices could be up one rate, down one rate, no change (as with the existing MVL) with the possible addition of a request for minimum rate or possibly some other indication such as a request for a retrain." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 5. "Next the sequencer configures multiplexer A to select the two bits representing the requested receive

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			rate (or retrain request) which are scrambled and encoded the same way and sent to the modulator via multiplexer C." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 7. "The signals that communicate changes in transmitted data rate, request for a change in received data rate (up, down, no change, minimum rate or retrain) and, for multipoint, the address of the polled tributary, are also sent with at least 3 dB of additional noise margin." Paradyne Patent Disclosure Form 799-0059-2 Revision Q, U.S. Provisional Application No. 60/150,436 at 8. "Robust communication of the transmit rate and the **optional maximum receive rate** in addition to elimination of unnecessary TC layer information contribute to efficient operation of the line." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 3. "Any station can indicate the <u>maximum rate at which it is able to receive data</u> in any transmission by

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			starting the transmit rate field of the PMD header with the escape symbol. This is then followed by two symbols to encode the transmit rate of payload data following the header and then by a second pair of symbols to encode the maximum rate at which this station is able to receive data. Since sending this information lengthen the header by 3 symbols the maximum receive rate indication is typically sent only when a station determines that the station to which it is now transmitting needs to update the maximum transmit rate value it is currently using. … Since outbound transmission typically contain ATM cells for more than one tributary, the ATU-C will normally use the lowest maximum receive rate indicated by all ATU-Rs" Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 4. "The first transmission by the ATU-C to each ATU-R following training would normally include the maximum receiver rate field." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 6.

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			"The signals that communicate changes in transmitted data rate, maximum received data rate, and the address of the polled tributary are also sent with at least 3 dB of additional noise margin." Broadband Tech Note 313, "Proposed Changes to MVL PMD Layer for ATM Transport", *submitted with* U.S. Provisional Application No. 60/150,436, at 7. *See also* '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment
9.	means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the	23(c), 24	Means plus function term: "means for encoding the preamble bits into a plurality of symbol indices". Function: Encoding the preamble bits into a plurality of symbol indices. Structure: A Preamble Encoder, or the equivalents. FIG. 8 (element 219) Intrinsic Support:	Means plus function element to be construed pursuant to 112, ¶ 6. Function – encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel (*See row 5 above* for construction of limitations of this function)

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maximum rate capable of being transmitted over a communication channel		FIG. 8, element 219; "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117. The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4)	<u>Structure</u> – **219**, the 2 bit per symbol preamble encoder <u>Intrinsic Support:</u> FIGS. 7-9 "FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. … The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117." 15:3-57. *See also* '444 patent file history at 1/5/04 Office Action; 3/19/04 Response & Amendment; 5/20/04 Office Action; 6/28/04 Response & Amendment; 11/19/04 Notice of Allowability; 2/22/05 Amendment After Notice of Allowance ; 8/22/05 Notice of Entry of Amendment *See row 5 above*

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		bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols, are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117." 15:3-28. "The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol." 7:15-23.	

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
1. first transmitting means in the transmitting modem, including adjusting means responsive to the pre-emphasis coefficients for adjusting frequency dependent characteristics of an output of said first transmitting means;	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 15, 16, 17, 18, 19, 20	Rembrandt does not believe this term requires construction. In the alternative: first transmitting means in the transmitting modem – a transmitter in the transmitting modem. Intrinsic Support: Fig. 5 and (element 14 and 16) "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." Col. 3, lines 46-58. including adjusting means responsive to the pre-	Means plus function element to be construed pursuant to 112, ¶ 6. Function – adjusting frequency dependent characteristics of an output of said first transmitting means Structure – conventional modem transmitter **14**, with nine-tap filter **70** comprising delay blocks **71-79**, multipliers **81-89**, and adder **90** Intrinsic Support: Figs. 5, 6. "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7 [sic, Fig. 6]." 3:47-54

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		emphasis coefficients for adjusting frequency dependent characteristics of an output of said first transmitting means – means plus function claim language to be construed pursuant to 112, ¶ 6 Means plus function term: "adjusting means". Function: Adjusting the frequency dependent characteristics of the output signal based upon the pre-emphasis coefficients. Structure: A pre-filter, or the equivalents. (Fig. 5 (element 16).) Intrinsic Support: Fig. 5, element 16; "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as	"Pre-filter 16 includes nine-tap filter 70 as shown in FIG. 6. Nine-tap filter 70 receives its input from the output from modem transmitter 14. The input is transmitted through a series of 9 delay blocks 71-79, the outputs of each of these delay blocks is sent through multipliers 81-89. Multipliers 81-89 receive their second multiplicands (C.sub.0 -C.sub.4) from compute block 48 and send their respective products to adder 90. The output of adder 90 is the output of pre-filter 16." 4:35-43. " . . . These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment.

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		shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." 3: 46-58; "These appropriate filter coefficients C.sub.i, i=0,4 are transmitted to pre-filter 16. However, pre-filter 16 implements these coefficients only whenever data is not being transmitted through pre-filter 16, such as just before a remote modem responds to a poll. This implementation precludes changing the transmission characteristics in the middle of a transmission." 5:22-28.	
2. adjusting frequency [dependent] characteristics	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 15, 16, 17, 18, 19, 20, 21(c)	Rembrandt does not believe this term requires construction. In the alternative: adjusting the frequency dependent characteristics. Intrinsic Support: Abstract; FIG. 5, element 16; "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present	adjusting the signal using pre-emphasis coefficients computed from the noise spectrum parameters, so that the signal to be input into the receiving modem has a constant signal to noise ratio across all frequencies whether the noise is injected before or after the high frequency roll-off of a communications line Intrinsic Support: FIGS. 1a, 1b, 1c, 2a, 2b, 2c, 3a, 3b and 3c; 4-6

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." 3:46-58; "These appropriate filter coefficients C.sub.i, i=0,4 are transmitted to pre-filter 16. However, pre-filter 16 implements these coefficients only whenever data is not being transmitted through pre-filter 16, such as just before a remote modem responds to a poll. This implementation precludes changing the transmission characteristics in the middle of a transmission." 5:22-28.	"FIG. 3a illustrates the received transmitter signal and the received noise both rolling off in parallel above break frequency w.sub.o. … However, prior art methods of pre-emphasis, either manual or automated, would look to the frequency dependent energy spectrum of the entire received signal (received transmitter signal plus received noise) and calculate a pre-emphasis similar to that shown in FIG. 2c. This would result in a lowering of the transmitter signal power and the signal to noise ratio at frequencies below break frequency Wo and an overall degradation in system performance. It is therefore the object of this invention to provide a method and apparatus for automated transmit pre-emphasis calculation which properly accounts for frequency-dependent signal-to-noise ratios." (2:15-44). "Field of Invention. This invention relates to an apparatus for determining a frequency-dependent signal-to-noise ratio in a communications network so as to allow proper equalization in a transmit pre-emphasis mode." (1:6-11)

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			"2. Description of the Prior Art It is well-known in the prior art that a transmitter in a communications network, particularly a multipoint network, should emphasize or amplify certain frequencies so as to compensate for frequency-dependent losses in the communications process." (1:12-17) "It is well-known in the prior art that a transmitter in a communications network, particularly a multipoint network, should emphasize or amplify certain frequencies so as to compensate for frequency-dependent losses in the communications process. For example, with the use of a telephone line as a communications line, losses are more pronounced at higher frequencies. These losses are typically modeled as a constant negative slope above a given break frequency on a decibels versus frequency plot." (1:13-22) "When noise is injected into a communications line subsequent to the high-frequency roll-off of the communications line and the signal rolls off above a break frequency while the noise signal remains

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			constant (thereby resulting in a signal-to-noise ratio which progressively decreases above the break frequency), prior art methods of frequency-dependent analysis of total energy received is adequate as an equalization technique." (1:23-30) "However, when noise is injected into a communications line prior to the high frequency roll-off of the communications line and the noise rolls off in parallel to the roll-off of the signals (resulting in a constant signal-to-noise ratio as a function of frequency), prior art methods of frequency-dependent analysis of total energy received are inadequate as an equalization technique." (1:37-44) "The ideal pre-emphasis, whether manually set or periodically calculated on-line, is illustrated in FIG. 2c wherein an increasing gain is applied above the frequency w.sub.o. This frequency-dependent pre-emphasis flattens the transmitter signal as received without affecting the noise signal, thereby increasing the signal-to-noise ratio at the frequencies above w.sub.o and improving overall system performance." (2:4-11) FIGS. 1a, 1b and 1c are illustrative of a

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			communications system with no frequency-dependent attenuation or roll-off. FIGS. 2a, 2b and 2c are illustrative of a communications system with noise injected subsequent to frequency-dependent attenuation or roll-off." (2:58-63) "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." (2:45-53) "Modem transmitter circuitry 10 includes analog-to-digital converter 44 and secondary channel receiver 46 which receives the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of

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			the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." (4:7-27) "The previous frequency spectrum is subtracted from the new frequency spectrum, and the result is divided in half. … Finally, these filter coefficients, C_i, $i=0,4$, are adjusted via an AGC circuit in compute block 48, so as to assure a constant power output from transmitting modem 10." (4:62-5:21) "These appropriate filter coefficients C_i, $i=0,4$ are transmitted to pre-filter 16." (5:21-22)

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U.S. Patent No. 5,008,903 **Claim Limitation**	Claims at Issue	REMBRANDT **CONSTRUCTION AND INTRINSIC EVIDENCE**	CABLE PARTIES **CONSTRUCTION AND INTRINSIC EVIDENCE**
			"The Martinez reference bases its equalization calculations upon information signals rather than upon noise signals. Moreover, the apparatus of this reference deals with amplitude and phase distortion rather than additive noise." (Response to Office Action, signed April 18, 1990, at 7) *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
3. receiving means for receiving said output from said first transmitting means	1(c), 2, 3, 4, 5, 6(c), 7, 8(c), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "receiving means" Function: Receiving output from the transmitting means. Structure: A receiver, or the equivalents. (Fig. 5 (element "RX", between elements 22 and 24)) Intrinsic Support: FIG. 5 (element "RX");	Means plus function element to be construed pursuant to 112, ¶ 6. Function – receiving said output from said first transmitting means Structure – analog-to-digital converter **22** Intrinsic Support: FIG. 5 "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into

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		"FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." 3:46-58; "The functional description of this invention is as follows. The transmitting modem 10 sends QAM modulated data signals to the receiving modem 12." 4:50-54.	digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described.." 3:59-68 *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
4. noise spectrum	1(d), 2, 3, 4, 5, 6(d), 7, 8(d), 15, 16, 17, 18, 19, 20,	Rembrandt does not believe this term requires construction. In the alternative: noise signal values. Intrinsic Support: Abstract; FIGS. 4, 5;	frequency domain plot of the noise signals across a range of frequencies Intrinsic Support: FIGS. 4-5

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	21(e)	"Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency. The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68." 3:30-41; "Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:42-46; File history, April 18, 1990 Amendment, Paper 8, pg 7.	"Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:41-46. "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a <u>frequency domain plot</u> of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by <u>discrete Fourier transform</u> techniques as previously described." 3:59-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from <u>a 22 point discrete Fourier transform calculation</u> so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office

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			Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
5. generating means for generating parameters responsive to a noise spectrum of said output	1(d), 2, 3, 4, 5, 8(d), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "generating means for generating parameters responsive to a noise spectrum of said output" Function: Generating parameters responsive to a noise spectrum of the output signal. Structure: A discrete Fourier transform circuit, or the equivalents. (FIG. 4 (68); Col. 3: 41-45; Col. 4: 55-56). Intrinsic Support: FIGS. 4, 5, "Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:42-46; "Analog-to-digital converter 22 (which corresponds	Means plus function element to be construed pursuant to 112, 6. Function – generating parameters by choosing points of a noise spectrum of said output Structure – noise spectrum generator circuit **50**, including complex DFT block **68** that calculates a frequency domain plot of the noise signal at 709, 1145, 1800, 2455 and 2891 Hertz chosen from a 22 point discrete Fourier transform Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its

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		to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:59-68; "In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26." 4:12-15.	own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:63-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. " . . . the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency

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			domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
6. generating means, including a noise spectrum generator circuit, for generating parameters responsive to a	6(d), 7	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "generating means for generating parameters responsive to a noise spectrum of said output"	Means plus function element to be construed pursuant to 112, 6. Function – generating parameters by choosing points of a noise spectrum of said output Structure – noise spectrum generator circuit **50**,

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noise spectrum of said output		Function: Generating parameters responsive to a noise spectrum of the output signal. Structure: Noise spectrum generator circuitry, or the equivalents. (Fig. 4, (element 50); FIG. 5 (element 24).) Intrinsic Support: "Noise spectrum generator circuit 50 includes analog-to-digital converters 52, 53 and sinusoidal mixers 54, 55 for demodulation. The demodulated signal from mixers 54, 55 is equalized by linear equalizers 56, 57. Linear equalizers 56, 57 are transversal filters which are from the prior art and are not to be confused with the equalization used for pre-emphasis in the transmitter circuitry. The resulting signals are phase corrected by phase corrector 60 which results in an x-y signal representative of the complex plane to slicer 62. Slicer 62 includes the constellation or eye pattern data which is used in the quadrature amplitude modulation scheme of the signal received by analog-to-digital convertors 52, 53. Slicer 62 outputs the constellation point which is closest to the input of slicer 62. Therefore, the actual received point is input to slicer 62 and the presumed	including complex DFT block **68** that calculates a frequency domain plot of the noise signal at 709, 1145, 1800, 2455 and 2891 Hertz chosen from a 22 point discrete Fourier transform Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously

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		actual transmitted point is output from slicer 62. Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency." The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68. Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:15-45.	described." 3:63-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum ($P.sub.i$, i=1,5) <u>of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation</u> so as to span the usable frequency of a telephone line." 4:54-60. " . . . the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum ($P'.sub.i$, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division

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			by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
7.	parameters responsive to a noise spectrum/ parameters responsive to said noise spectrum	1, 6, 8, 21	Values based upon the noise signal at given frequencies. Intrinsic Support: FIG. 4, element 50, 68; FIG. 5, element 24; "Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:42-46; "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum	Means plus function element to be construed pursuant to 112, 6. Function – generating parameters by choosing points of a noise spectrum of said output Structure – noise spectrum generator circuit **50**, including complex DFT block **68** that calculates a frequency domain plot of the noise signal at 709, 1145, 1800, 2455 and 2891 Hertz chosen from a 22 point discrete Fourier transform Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum

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		analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:59-68; File history, April 18, 1990 Amendment, Paper 8, pg 7.	generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:63-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) <u>of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation</u> so as to span the usable frequency of a telephone line." 4:54-60.

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			" . . . the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment

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8. said parameters	1(e), 2, 3, 4, 5, 6(e), 7, 8(e), 15, 16, 17, 18, 19, 20, 21(g)	Rembrandt does not believe this term requires construction. In the alternative: values based upon the noise spectrum [defined above]. Intrinsic Support: "Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10." 4:1-6; "The spectrum is transmitted back to the transmitting modem 10 over the secondary channel." 4:60-62.	generated parameters chosen as points of a noise spectrum of said output Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:63-68

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			"The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. " . . . the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention.

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			The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
9. generating parameters responsive to said noise spectrum of said output	21(f)	Rembrandt does not believe this term requires construction. In the alternative: generating values based upon the noise spectrum [defined above] of the signal received from the transmitting modem. Intrinsic Support: Figs. 4 and 5 and "The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68. Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." Col. 3, lines 37-45;	generating parameters by choosing points of a noise spectrum of said output Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53.

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		"In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26." 4:12-15; "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." lines 58-67. (see above.) "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." Col. 4, lines 54-61.	"The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:63-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. " . . . the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division

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			is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
<u>10.</u> means for calculating said noise spectrum of said output	1(d), 2, 3, 4, 5, 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. <u>Means plus function term</u>: "means for calculating said noise spectrum of said output". <u>Function</u>: Calculating said noise spectrum of said output. <u>Structure</u>: Noise spectrum generator circuitry, or the equivalents. (Fig. 4, (element 50); FIG. 5 (element	Means plus function element to be construed pursuant to 112, 6. <u>Function</u> – calculating noise signals of said output in the time domain and converting them into a spectrum in the frequency domain <u>Structure</u> – noise spectrum generator circuit **50**, including equalizers **56** & **57**, phase corrector **60**, slicer **62**, comparator **64**, inverse phase corrector **66** and block **68** that performs a 22 point discrete Fourier

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		24).) Intrinsic Support: FIGS. 4, 5; "Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency. The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68." 3:30-41.	transformation calculation Intrinsic Support: FIGS. 4-5 "Noise spectrum generator circuit 50 includes analog-to-digital converters 52, 53 and sinusoidal mixers 54, 55 for demodulation. The demodulated signal from mixers 54, 55 is equalized by linear equalizers 56, 57. Linear equalizers 56, 57 are transversal filters which are from the prior art and are not to be confused with the equalization used for pre-emphasis in the transmitter circuitry. The resulting signals are phase corrected by phase corrector 60 which results in an x-y signal representative of the complex plane to slicer 62. Slicer 62 includes the constellation or eye pattern data which is used in the quadrature amplitude modulation scheme of the signal received by analog-to-digital convertors 52, 53. Slicer 62 outputs the constellation point which is closest to the input of slicer 62. Therefore, the actual received point is input to slicer 62 and the presumed actual transmitted point is output from slicer 62. Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is

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			representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency. The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68. Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:14-46. "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of

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11. noise spectrum generator circuit	6(g), 7, 8(g)	Rembrandt does not believe this term requires construction. In the alternative: circuitry that generates a noise spectrum [defined above]. Intrinsic Support: FIGS. 4, 5; "Noise spectrum generator circuit 50 includes analog-to-digital converters 52, 53 and sinusoidal mixers 54, 55 for demodulation. The demodulated signal from mixers 54, 55 is equalized by linear equalizers 56, 57. Linear equalizers 56, 57 are transversal filters which are from the prior art and are not to be confused with the equalization used for pre-emphasis in the transmitter circuitry. The resulting signals are phase corrected by phase corrector 60 which results in an x-y signal representative of the complex plane to slicer 62. Slicer 62 includes the constellation or eye pattern data which is used in the quadrature amplitude modulation scheme of the signal received by analog-to-digital convertors 52, 53. Slicer 62 outputs the constellation point which is closest to the input of slicer 62. Therefore, the actual	circuit which calculates noise signals in the time domain (successive values corresponding to successive frequencies) and converts them into a spectrum in the frequency domain and generates parameters by choosing points of the noise spectrum Intrinsic Support: FIGS 4, 5 "Noise spectrum generator circuit 50 includes analog-to-digital converters 52, 53 and sinusoidal mixers 54, 55 for demodulation. … Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:14-46. "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to

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		received point is input to slicer 62 and the presumed actual transmitted point is output from slicer 62. Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency." The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68. Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:15-46 "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum analysis block 24. The remainder of the noise	compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:63-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment

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		spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:59-68; File history, April 18, 1990 Amendment, Paper 8, pg 7.	
12.	calculating a noise spectrum of said output	21(e)	Rembrandt does not believe this term requires construction. In the alternative: calculating a noise spectrum [defined above] of the signal received from the transmitting modem. Intrinsic Support: FIGS. 4, 5; "Comparator 64 subtracts the actual received point from the actual transmitted point so as to calculate an error signal which is representative of the noise signal at the given frequency. This error or noise signal is inversely related to the distance between the signal line and the noise line of FIGS, 1 a, 2a and 3a at the given frequency.	calculating noise signals of said output in the time domain and converting them into a spectrum in the frequency domain Intrinsic Support: FIGS. 4-5 "Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:41-46. "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into

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		The resulting error signal is phase corrected by inverse phase corrector 66. The output of inverse phase corrector 66 is used to update the characteristics of linear equalizers 56, 57 and as an input to complex DFT (discrete Fourier transform) block 68." 3:30-41; "Complex DFT block 68 converts the phase corrected noise signals in the time domain (i.e. successive values corresponding to successive frequencies) into the noise spectrum in the frequency domain." 3:42-46; "Analog-to-digital converter 22 (which corresponds to analog-to-digital converters 42, 43 of FIG. 4) converts the analog signal from communications line 20 into digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a frequency domain plot of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by discrete Fourier transform techniques as previously described." 3:59-68; File history, April 18, 1990 Amendment, Paper 8, pg	digital format for input into noise spectrum analysis block 24. The remainder of the noise spectrum generator circuit of FIG. 4 is included in noise spectrum analysis block 24 from which a <u>frequency domain plot</u> of the noise signal (P'.sub.i, i=1,5) is output, said frequency domain plot being derived by <u>discrete Fourier transform</u> techniques as previously described." 3:59-68 "The noise spectrum generator circuit 50, including the complex DFT block 68, calculates a frequency spectrum (P.sub.i, i=1,5) of the noise at 5 frequencies--709, 1145, 1800, 2455 and 2891 Hertz. These frequencies are chosen from <u>a 22 point discrete Fourier transform calculation</u> so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment

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		7.	
13. second transmitting means for transmitting said parameters to the transmitting modem	1(e), 2, 3, 4, 5, 6(e), 7, 8(e), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "second transmitting means". Function: Transmitting said parameters to the transmitting modem. Structure: A second transmitter, or the equivalents. (Fig. 5 (element 38).) Intrinsic Support: Abstract; FIG. 5; "Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10." 4:1-6;	Means plus function element to be construed pursuant to 112, 6. Function – transmitting said parameters to the transmitting modem Structure – low rate secondary channel transmitter **38** that transmits on a sideband of the primary channel at a low transmission rate through line **42** Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53.

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		"The spectrum is transmitted back to the transmitting modem 10 over the secondary channel." 4:60-62.	"Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10." 4:1-6. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment

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14. secondary channel	15, 16	A second communication path provided by a transmission medium via either physical or electrical separation from a first communication path. Intrinsic Support: Abstract; Fig. 5; "Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10."4:1-6; "The spectrum is transmitted back to the transmitting modem 10 over the secondary channel." 4:60-62.	sideband of the primary channel *See row 13 above* Intrinsic Support: FIGS. 4-5 "This apparatus and method uses a noise spectrum generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10." 4:1-6.

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15. computing means for computing the pre-emphasis coefficients from said parameters	1(f), 2, 3, 4, 5, 6(f), 7, 8(f), 15, 16, 17, 18, 19, 20	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "computing means". Function: Computing the pre-emphasis coefficients from the parameters. Structure: compute/computer block 48 and operating code which performs the steps of computing the pre-emphasis coefficients from the parameters, or the equivalents. (Fig. 4 (element 48); Col. 4: 66, Col. 5: 17.) Intrinsic Support: FIGS. 4, 5; "The output of multiplier 30 is input to compute block 48 which calculates and transmits the pre-filter coefficients (C.sub.i, i=0,4) for pre-filter 16 as will	Means plus function element to be construed pursuant to 112, 6. Function – computing at the transmitting modem pre-emphasis coefficients from said parameters Structure – transmitting modem circuitry containing comparator **28** that subtracts the previous frequency domain plot of the noise signal (previous parameters) stored in shift register **26** from the current plot (current parameters), multiplier **30** that divides the output of the comparator, compute block **48** implementing the log to linear algorithm at Col. 4:66 and the algorithms set forth at Col. 5:1-17; and including AGC circuit Intrinsic Support: FIGS. 5; 6 "This apparatus and method uses a noise spectrum

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		be described hereinafter." 4:31-34; "The frequency spectrum (P.sub.i, i=1,4) of the noise expressed in a logarithm scale are converted to a linear scale (F.sub.i, i=0,4) in compute block 48. The linear scale frequency spectrum is converted to filter coefficients through the following transformation: ##EQU1## C.sub.i, i=0,4, is then transformed by computer block 48 into C'.sub.i, i=0,4 in order to adjust the pre-emphasis coefficients to be appropriate for the resonators of the resonating filters. These resonators are located at 0, 600, 1200 and 2400 Hertz. An iterative calculation is done to adjust the pre-emphasis coefficients, C'.sub.i, i=0,4 (i.e. scalars) into appropriate filter coefficients, C.sub.i, i=0,4. Finally, these filter coefficients, C.sub.i, i=0,4, are adjusted via an AGC circuit in compute block 48, so as to assure a constant power output from transmitting modem 10. These appropriate filter coefficients C.sub.i, i=0,4 are transmitted to pre-filter 16. However, pre-filter 16 implements these coefficients only whenever data is not being transmitted through pre-filter 16, such as just before a remote modem responds to a poll. This	generator circuit to calculate a frequency-dependent noise spectrum. This spectrum is transmitted from the receiver to the transmitter (or from the master to the remote in a multipoint system) via the secondary channel. The transmitter uses this information to compute the new pre-emphasis coefficients from its own transmitted spectrum as seen by the receiver and uses the result on its subsequent transmission." 2:45-53. "Secondary channel transmitter 38 transmits communications network control parameters, including the spectrum (P.sub.i, i=1,5) from block 24, on a sideband of the primary channel at a low transmission rate through line 42 via digital-to-analog converter 40 to analog-to-digital converter 44 of modem transmitter circuitry 10." 4:1-6. "Modem transmitter circuitry 10 includes analog-to-digital converter 44 and secondary channel receiver 46 which receives the spectrum sent from secondary channel transmitter 38 through line 42. Secondary channel receiver 46 transmits the spectrum (P'.sub.i, i=1,5) data to comparator 28. In order to account for existing pre-emphasis, the frequency domain plot of the noise signal has subtracted from it the previous

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		implementation precludes changing the transmission characteristics in the middle of a transmission." 4:66-5:28.	frequency domain plot as stored in shift register 26. This subtraction is performed by comparator 28. The reference spectrum outputs from comparator 28 is multiplied by one half by multiplier 30. This division is done as the current state-of-the-art is to have the transmitter provide by pre-emphasis one half of the signal compensation required while the receiver provides the other half. The portion provided by the receiver of, course, is done by apparatus separate from the invention as herein described. This division by two is optional and not crucial to the invention. The reference spectrum may be divided by other values, or not divided at all, in other embodiments of the invention." 4:7-27. "The previous frequency spectrum is subtracted from the new frequency spectrum, and the result is divided in half . . . The frequency spectrum . . . of the noise expressed in a logarithm scale are converted to a linear scale . . . The linear scale frequency spectrum is converted to filter coefficients through the following transformation . . . Finally, these filter coefficients, C.sub.i, i=0,4, are adjusted via an AGC circuit in compute block 48, so as to assure a constant power output from transmitting modem 10." 4:62-5:21.

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			See also '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment
<u>16.</u> output from said transmitting step	21(c)	Rembrandt does not believe this term requires construction. In the alternative: output signal from the transmitting modem. <u>Intrinsic Support:</u> FIG. 5; "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." 3:46-57	output of modem transmitter to be adjusted responsive to the pre-emphasis coefficients <u>Intrinsic Support:</u> Figs. 5, 6. "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7 [sic, Fig. 6]." 3:47-54 "Pre-filter 16 includes nine-tap filter 70 as shown in FIG. 6. Nine-tap filter 70 receives its input from the output from modem transmitter 14. The input is transmitted through a series of 9 delay blocks 71-79, the outputs of each of these delay blocks is sent

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			through multipliers 81-89. Multipliers 81-89 receive their second multiplicands (C.sub.0 -C.sub.4) from compute block 48 and send their respective products to adder 90. The output of adder 90 is the output of pre-filter 16." 4:35-43. " . . . These frequencies are chosen from a 22 point discrete Fourier transform calculation so as to span the usable frequency of a telephone line." 4:54-60. *See also* '903 patent file history at 1/5/90 Office Action; 4/23/90 Amendment; 7/24/90 Notice of Allowability & Amendment.
17.	receiving said output from said first transmitting means	21(d)	Rembrandt does not believe this term requires construction. In the alternative: receiving the output signal sent from the transmitting modem. Intrinsic Support: FIG. 5; "FIG. 5 discloses the entire modem transmitter circuit 10 and modem receiver circuit 12 of the present invention. Modem transmitter circuit 10 includes a conventional modem transmitter 14 which outputs digital signals to be transmitted to pre-filter 16. Pre-filter 16 pre-emphasizes the digital	remote modem receives said output from said first transmitting means Intrinsic Support: *See row 16 above*

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		signals prior to their conversion to analog signals. Pre-filter 16, as will be described herein, includes nine-tap filter 70 as shown in FIG. 7. The output of the pre-filter 16 is converted to analog format by digital-to-analog converter 18 for transmission across communications line 20, which may be a telephone line, to modem receiver circuit 12." 3:46-57	

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1. said memory being of a type which may be completely updated in its entirety but which is not volatile	1(b), 2, 3, 4, 5	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten. Intrinsic Support: "Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." 4:17-21. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other)…." 4: 21-27. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20;	the system enables all contents in the system's non-volatile memory to be erased and overwritten during an update Intrinsic Support: FIGS. 1-3. "In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded." Abstract. "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:3-5. "Stored program controlled apparatus can

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		3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:28-36. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." 4:15-18. "In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:1-5. '159 Patent File History, Papers 1, 2, 4, 15-18, 21,	conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled"." 1:6-10. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. **"In accordance with the principles of this invention, the <u>entire set of programs</u> contained in memory 20 can be <u>over-written</u> with a new set of programs…"** 3:47-49. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks

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		24-26, 29, 31. FIGS. 1-3.	(distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves." 4:21-27. **"To summarize the downloading process of this invention,** **1. Bulk erase … that half of memory 20 which does NOT contain the EP set of programs; …** **4. Bulk erase the other half of memory 20[.]"** 4:28-35. **"1. Bulk erase the second half of memory 20; …** **5. bulk erase the first half of memory 20[.]."** 4:49-55. "In particular, by storing all programs, including the initialization program, in EEPROM, and by providing a means by which two events can occur -- namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs -- it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the

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			initialization program, all without requiring storage of any program information (including any initialization program information) in a non-writeable (ROM) device." File History, Sept. 30, 1997 Amendment, p. 3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized." File History, Sept. 30, 1997 Amendment, p. 5. "The present invention provides a unique approach to solving a problem which is present in a number of microprocessor based devices, i.e., the inability to upgrade all the firmware of the device in the field…. In particular, by storing all programs, including the initialization program, in EEPROM which can be written to by the user, and by providing a means by which two events can occur – namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the

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			initialization program and main programs – it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a nonwriteable memory. As will be illustrated below, unlike the present invention, *Beaverton* requires the storage of certain program information in a nonwriteable memory and is, therefore, clearly distinguishable from the present invention. The present invention, as defined by independent claims 1, 6, 8, 13 [issued 10] and 22 [issued 18], includes a memory which is required to be non-volatile and <u>capable of being updated</u>." [applicant's underscore] File History, Jan. 20, 1998 Amendment, pp.3-4, remarks re all independent claims. "Like the present invention, *Beaverton* teaches a system in which all of the memory is EEPROM. However, in contrast to the present invention, *Beaverton* specifically "provides for the firmware resident in the EEPROM to be hardware partitioned into protected and unprotected areas. **The**

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			partitioning of the firmware prevents a user from writing over selected partitions of the firmware resident in the EEPROM. This insures that a minimum amount of firmware is constant in the system . . ." (*Beaverton*, col. 2, lines 51-57) (emphasis added [by applicant]). "The invention [in *Beaverton*] provides a control logic device to maintain a preselected amount of firmware in a protected partition to prevent overwriting **by the user** . . ." (*Beaverton*, col. 3, lines 30-33) (emphasis added [by applicant]). The EEPROM memory in *Beaverton* is partitioned into three ranges, a writeable range, a conditionally rewriteable range, and a protected (nonwriteable) range. (*Beaverton*, col. 5, lines 16-68; col. 6, lines 1-14; FIGS. 3 and 4). "The lower address range (20040000 to [20041FFF]) partition 37 is a nonwriteable partition reserved for the firmware entry code that can never be written to **by a user**." (*Beaverton*, col. 5, lines 67-68; col. 6, lines 1-2) (emphasis added [applicant's underscore]). This limitation makes clear that *Beaverton* does not contain al the elements of the present invention in that ***Beaverton's* partitioned and partially protected (i.e., nonwriteable) "memory" is not the same element as the "memory" of the present invention,**

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			which is capable of being updated. By prohibiting the user from writing over certain portions of the firmware, *Beaverton* clearly did not consider the possibility of the present invention, **namely the ability of a user to update <u>all</u> of the firmware in the system *by overwriting* the memory containing such firmware. [applicant's underscore]** To summarize, the concept of the present invention, namely to be able to change all the programs in the system, including the initialization programs, was not mentioned in *Beaverton* and, in fact, is specifically prohibited by *Beaverton*. The inventors in *Beaverton* knew of (and used) non-volatile EEPROMs as their system memory, but required partitioning of the memory and storage of their firmware entry code in a nonwriteable portion of the EEPROM. This clearly shows that their invention does not anticipate **the use of a memory which can be completely overwritten** so that **all** the programs in the system, including the system initialization programs, can be updated by writing new programs into the memory. **By prohibiting the user from writing to certain portions of its system memory, *Beaverton*, in fact, teaches away from the present invention.**" File History, Jan. 20, 1998 Amendment, pp.5-6, remarks

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			independent claims 1, 6, 8 and 22 [issued 18]. "Both *Beaverton* and *Ahlin* teach a system having a memory that has a non-writeable portion. There is nothing in those patents that can be combined to remove the limitation that a portion of the memory must be non-writeable. **Likewise, neither *Beaverton* nor *Ahlin*, alone or in combination, teach a system having a memory that is capable of being fully updated**, including the updating of the system initialization programs, through a communications port." File History, Jan. 20, 1998 Amendment, p. 9. "(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a [single] type which may be <u>completely</u> updated <u>in its entirety</u> but which is not volatile, said memory being the only program memory in said system" (Note that this amendment was submitted because the applicant's 1/2/98 Remarks alone were considered insufficient) File History, Apr. 2, 1998 Amendment, p.2, re claim 1. "Applicants believe that Beaverton teaches a system for updating programs stored in an EEPROM by

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			storing a new sub-routine into a new location on an EEPROM, and then updating a second transfer vector identifying the starting address of the new subroutine. However, in Beaverton, at least one program portion resides in a *protected* partition within the EEPROM and other program portions reside in an unprotected partition within the EEPROM. Program software in Beaverton can only be loaded onto the *unprotected* partition of the EEPROM (column 3, lines 1-9). Beaverton provides that the protected partition of the EEPROM is a "non-writable partition reserve for the firmware entry code that can never be written to by a user." (See column 5, line 67 to column 6, line 2.) [applicant's emphasis] In contrast, the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications … are downloadable. That is, the apparatus of employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only memory" (page 3, lines 9-13). Applicants, therefore, respectfully submit that there are no teachings in Kreifels (which Applicants believe to merely teach an apparatus and method for the

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			writing to and the erasing of an EEPROM memory device) to combine with the teachings of Beaverton (which Applicants believe to teach program software residing in an EEPROM with **a portion of the software residing in a protected, non-writeable partition) t**o arrive at the Applicants' present invention, which teaches at least the elements of an initialization program residing in a memory in which the initialization program may be completely updated in its entirety. More specifically, claim 1 recites the limitation of "a memory being of a type which may be completely updated in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Claim 6 recites the limitation of a "memory being completely updatable in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Furthermore, claim 22 recites the limitation of a "memory being of a type which is completely updatable in its entirety" and "a set of program means stored in said memory that are activated when said system needs to be updated." … In addition, a reference "teaches away" from the

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			claimed invention and should not be used to reject the claimed invention under §103 "when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." … **Applicants believe that one of the critical inventive steps in Beaverton is that a non-writable partition provides security for the initialization program. Therefore, Applicants submit that a person of ordinary skill, when applying Beaverton's apparatus and method, <u>would not be directed to erasing the entire initialization program as the Applicants teach and claim.</u>**" File History, Feb. 23, 2000 Amendment, p.3-4, remarks re independent claims 1, 6 and 22 [issued 18].
<u>2.</u> said memory being completely updatable in its entirety but non-volatile	6(b), 7, 8(b), 9	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten. Intrinsic Support: See support cited for construction of said memory being of a type which may be completely updated in	the system enables all contents in the system's non-volatile memory to be erased and overwritten during an update Intrinsic Support: FIGS. 1-3.

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		its entirety but which is not volatile	"In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded." Abstract. "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:3-5. "Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled"." 1:6-10.

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			"The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. **"In accordance with the principles of this invention, the <u>entire set of programs</u> contained in memory 20 can be <u>over-written</u> with a new set of programs…"** 3:47-49. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves." 4:21-27. **"To summarize the downloading process of this invention,** **1. Bulk erase … that half of memory 20 which does NOT contain the EP set of programs; …**

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			4. Bulk erase the other half of memory 20[.]" 4:28-35. **"1. Bulk erase the second half of memory 20; … 5. bulk erase the first half of memory 20[.]."** 4:49-55. "In particular, by storing all programs, including the initialization program, in EEPROM, and by providing a means by which two events can occur -- namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs -- it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a non-writeable (ROM) device." File History, Sept. 30, 1997 Amendment, p. 3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which

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			may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized." File History, Sept. 30, 1997 Amendment, p. 5. "The present invention provides a unique approach to solving a problem which is present in a number of microprocessor based devices, i.e., the inability to upgrade all the firmware of the device in the field…. In particular, by storing all programs, including the initialization program, in EEPROM which can be written to by the user, and by providing a means by which two events can occur – namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs – it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a nonwriteable memory. As will be illustrated below, unlike the present invention, *Beaverton* requires the storage of certain program

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			information in a nonwriteable memory and is, therefore, clearly distinguishable from the present invention. The present invention, as defined by independent claims 1, 6, 8, 13 [issued 10] and 22 [issued 18], includes a memory which is required to be non-volatile and <u>capable of being updated</u>." [applicant's underscore] File History, Jan. 20, 1998 Amendment, pp.3-4, remarks re all independent claims. "Like the present invention, *Beaverton* teaches a system in which all of the memory is EEPROM. However, in contrast to the present invention, *Beaverton* specifically "provides for the firmware resident in the EEPROM to be hardware partitioned into protected and unprotected areas. **<u>The partitioning of the firmware prevents a user from writing over selected partitions of the firmware resident in the EEPROM.</u>** This insures that a minimum amount of firmware is constant in the system . . ." (*Beaverton*, col. 2, lines 51-57) (emphasis added [by applicant]). "The invention [in *Beaverton*] provides a control logic device to maintain a preselected amount of firmware in a protected partition <u>to prevent overwriting</u> **by the user** . . ."

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			(*Beaverton*, col. 3, lines 30-33) (emphasis added [by applicant]). The EEPROM memory in *Beaverton* is partitioned into three ranges, a writeable range, a conditionally rewriteable range, and a protected (nonwriteable) range. (*Beaverton*, col. 5, lines 16-68; col. 6, lines 1-14; FIGS. 3 and 4). "The lower address range (20040000 to [20041FFF]) partition 37 is a nonwriteable partition reserved for the firmware entry code that can never be written to **by a user**." (*Beaverton*, col. 5, lines 67-68; col. 6, lines 1-2) (emphasis added [applicant's underscore]). This limitation makes clear that *Beaverton* does not contain al the elements of the present invention in that ***Beaverton's* partitioned and partially protected (i.e., nonwriteable) "memory" is not the same element as the "memory" of the present invention, which is capable of being updated.** By prohibiting the user from writing over certain portions of the firmware, *Beaverton* clearly did not consider the possibility of the present invention, **namely the ability of a user to update all of the firmware in the system *by overwriting* the memory containing such firmware. [applicant's underscore]** To summarize, the concept of the present invention,

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			namely to be able to change all the programs in the system, including the initialization programs, was not mentioned in *Beaverton* and, in fact, is specifically prohibited by *Beaverton*. The inventors in *Beaverton* knew of (and used) non-volatile EEPROMs as their system memory, but required partitioning of the memory and storage of their firmware entry code in a nonwriteable portion of the EEPROM. This clearly shows that their invention does not anticipate **the use of a memory which can be completely overwritten** so that **all** the programs in the system, including the system initialization programs, can be updated by writing new programs into the memory. **By prohibiting the user from writing to certain portions of its system memory, *Beaverton*, in fact, teaches away from the present invention.** " File History, Jan. 20, 1998 Amendment, pp.5-6, remarks independent claims 1, 6, 8 and 22 [issued 18]. "Both *Beaverton* and *Ahlin* teach a system having a memory that has a non-writeable portion. There is nothing in those patents that can be combined to remove the limitation that a portion of the memory must be non-writeable. **Likewise, neither *Beaverton* nor *Ahlin*, alone or in combination, teach a system having a memory that is capable of being fully**

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			updated, including the updating of the system initialization programs, through a communications port." File History, Jan. 20, 1998 Amendment, p. 9. "(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a [single] type which may be <u>completely</u> updated <u>in its entirety</u> but which is not volatile, said memory being the only program memory in said system" (Note that this amendment was submitted because the applicant's 1/2/98 Remarks alone were considered insufficient) File History, Apr. 2, 1998 Amendment, p.2, re claim 1. "Applicants believe that Beaverton teaches a system for updating programs stored in an EEPROM by storing a new sub-routine into a new location on an EEPROM, and then updating a second transfer vector identifying the starting address of the new subroutine. However, in Beaverton, at least one program portion resides in a *protected* partition within the EEPROM and other program portions reside in an unprotected partition within the EEPROM. Program software in Beaverton can only be loaded onto the *unprotected* partition of the EEPROM (column 3, lines 1-9).

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			Beaverton provides that the protected partition of the EEPROM is a "non-writable partition reserve for the firmware entry code that can never be written to by a user." (See column 5, line 67 to column 6, line 2.) [applicant's emphasis] In contrast, the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications … are downloadable. That is, the apparatus of employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only memory" (page 3, lines 9-13). Applicants, therefore, respectfully submit that there are no teachings in Kreifels (which Applicants believe to merely teach an apparatus and method for the writing to and the erasing of an EEPROM memory device) to combine with the teachings of Beaverton (which Applicants believe to teach program software residing in an EEPROM with **a portion of the software residing in a protected, non-writeable partition) t**o arrive at the Applicants' present invention, which teaches at least the elements of an initialization program residing in a memory in which the initialization program may be completely updated

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			in its entirety. More specifically, claim 1 recites the limitation of "a memory being of a type which may be completely updated in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Claim 6 recites the limitation of a "memory being completely updatable in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Furthermore, claim 22 recites the limitation of a "memory being of a type which is completely updatable in its entirety" and "a set of program means stored in said memory that are activated when said system needs to be updated." … In addition, a reference "teaches away" from the claimed invention and should not be used to reject the claimed invention under §103 "when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." … **Applicants believe that one of the critical inventive steps in Beaverton is that a non-writable partition provides security for the initialization program.**

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			Therefore, Applicants submit that a person of ordinary skill, when applying Beaverton's apparatus and method, <u>would not be directed to erasing the entire initialization program as the Applicants teach and claim.</u>" File History, Feb. 23, 2000 Amendment, p.3-4, remarks re independent claims 1, 6 and 22 [issued 18].
<u>3.</u>	said memory being non-volatile and capable of being completely updated in its entirety	10(c), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory which may be overwritten. Intrinsic Support: Intrinsic Support: "Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." 4:17-21. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other)…." 4: 21-27.	the system enables all contents in the system's non-volatile memory to be erased and overwritten during an update Intrinsic Support: FIGS. 1-3. "In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded." Abstract.

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		"To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:28-36. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." 4:15-18.	"This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:3-5. "Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled"." 1:6-10. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. **"In accordance with the principles of this invention, the <u>entire set of programs</u> contained in**

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		"In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:1-5. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31. FIGS. 1-3.	**memory 20 can be <u>over-written</u> with a new set of programs…"** 3:47-49. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves." 4:21-27. **"To summarize the downloading process of this invention,** **1. Bulk erase … that half of memory 20 which does NOT contain the EP set of programs; …** **4. Bulk erase the other half of memory 20[.]"** 4:28-35. **"1. Bulk erase the second half of memory 20; …** **5. bulk erase the first half of memory 20[.]."** 4:49-55. "In particular, by storing all programs, including the initialization program, in EEPROM, and by providing a means by which two events can occur -- namely, the

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			partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs -- it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a non-writeable (ROM) device." File History, Sept. 30, 1997 Amendment, p. 3.

"The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized." File History, Sept. 30, 1997 Amendment, p. 5.

"The present invention provides a unique approach to solving a problem which is present in a number of microprocessor based devices, i.e., the inability to upgrade all the firmware of the device in the field…. |

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			In particular, by storing all programs, including the initialization program, in EEPROM which can be written to by the user, and by providing a means by which two events can occur – namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs – it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a nonwriteable memory. As will be illustrated below, unlike the present invention, *Beaverton* requires the storage of certain program information in a nonwriteable memory and is, therefore, clearly distinguishable from the present invention. The present invention, as defined by independent claims 1, 6, 8, 13 [issued 10] and 22 [issued 18], includes a memory which is required to be non-volatile and capable of being updated." [applicant's underscore] File History, Jan. 20, 1998 Amendment, pp.3-4, remarks re all independent claims.

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U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			"Like the present invention, *Beaverton* teaches a system in which all of the memory is EEPROM. However, in contrast to the present invention, *Beaverton* specifically "provides for the firmware resident in the EEPROM to be hardware partitioned into protected and unprotected areas. **The partitioning of the firmware prevents a user from writing over selected partitions of the firmware resident in the EEPROM.** This insures that a minimum amount of firmware is constant in the system . . ." (*Beaverton*, col. 2, lines 51-57) (emphasis added [by applicant]). "The invention [in *Beaverton*] provides a control logic device to maintain a preselected amount of firmware in a protected partition to prevent overwriting **by the user** . . ." (*Beaverton*, col. 3, lines 30-33) (emphasis added [by applicant]). The EEPROM memory in *Beaverton* is partitioned into three ranges, a writeable range, a conditionally rewriteable range, and a protected (nonwriteable) range. (*Beaverton*, col. 5, lines 16-68; col. 6, lines 1-14; FIGS. 3 and 4). "The lower address range (20040000 to [20041FFF]) partition 37 is a nonwriteable partition reserved for the firmware entry code that can never be written to **by a user**." (*Beaverton*, col. 5, lines 67-68; col. 6, lines 1-2)

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			(emphasis added [applicant's underscore]). This limitation makes clear that *Beaverton* does not contain al the elements of the present invention in that ***Beaverton's* partitioned and partially protected (i.e., nonwriteable) "memory" is not the same element as the "memory" of the present invention, which is capable of being updated.** By prohibiting the user from writing over certain portions of the firmware, *Beaverton* clearly did not consider the possibility of the present invention, **namely the ability of a user to update <u>all</u> of the firmware in the system *by overwriting* the memory containing such firmware. [applicant's underscore]** To summarize, the concept of the present invention, namely to be able to change all the programs in the system, including the initialization programs, was not mentioned in *Beaverton* and, in fact, is specifically prohibited by *Beaverton*. The inventors in *Beaverton* knew of (and used) non-volatile EEPROMs as their system memory, but required partitioning of the memory and storage of their firmware entry code in a nonwriteable portion of the EEPROM. This clearly shows that their invention does not anticipate **the use of a memory which can be completely overwritten**

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			so that **all** the programs in the system, including the system initialization programs, can be updated by writing new programs into the memory. **By prohibiting the user from writing to certain portions of its system memory, *Beaverton*, in fact, teaches away from the present invention.** " File History, Jan. 20, 1998 Amendment, pp.5-6, remarks independent claims 1, 6, 8 and 22 [issued 18]. "Both *Beaverton* and *Ahlin* teach a system having a memory that has a non-writeable portion. There is nothing in those patents that can be combined to remove the limitation that a portion of the memory must be non-writeable. **Likewise, neither *Beaverton* nor *Ahlin*, alone or in combination, teach a system having a memory that is capable of being fully updated**, including the updating of the system initialization programs, through a communications port." File History, Jan. 20, 1998 Amendment, p. 9. "(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a [single] type which may be <u>completely</u> updated <u>in its entirety</u> but which is not volatile, said memory being the only program memory in said system" (Note that this

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			amendment was submitted because the applicant's 1/2/98 Remarks alone were considered insufficient) File History, Apr. 2, 1998 Amendment, p.2, re claim 1.

"Applicants believe that Beaverton teaches a system for updating programs stored in an EEPROM by storing a new sub-routine into a new location on an EEPROM, and then updating a second transfer vector identifying the starting address of the new subroutine. However, in Beaverton, at least one program portion resides in a *protected* partition within the EEPROM and other program portions reside in an unprotected partition within the EEPROM. Program software in Beaverton can only be loaded onto the *unprotected* partition of the EEPROM (column 3, lines 1-9). Beaverton provides that the protected partition of the EEPROM is a "non-writable partition reserve for the firmware entry code that can never be written to by a user." (See column 5, line 67 to column 6, line 2.) [applicant's emphasis]

In contrast, the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications … are downloadable. That is, the apparatus of employing the |

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			principles of this invention does not need to have a non-volatile 'boot-up' read-only memory" (page 3, lines 9-13). Applicants, therefore, respectfully submit that there are no teachings in Kreifels (which Applicants believe to merely teach an apparatus and method for the writing to and the erasing of an EEPROM memory device) to combine with the teachings of Beaverton (which Applicants believe to teach program software residing in an EEPROM with **a portion of the software residing in a protected, non-writeable partition) t**o arrive at the Applicants' present invention, which teaches at least the elements of an initialization program residing in a memory in which the initialization program may be completely updated in its entirety. More specifically, claim 1 recites the limitation of "a memory being of a type which may be completely updated in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Claim 6 recites the limitation of a "memory being completely updatable in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			initialized." Furthermore, claim 22 recites the limitation of a "memory being of a type which is completely updatable in its entirety" and "a set of program means stored in said memory that are activated when said system needs to be updated." … In addition, a reference "teaches away" from the claimed invention and should not be used to reject the claimed invention under §103 "when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." … **Applicants believe that one of the critical inventive steps in Beaverton is that a non-writable partition provides security for the initialization program. Therefore, Applicants submit that a person of ordinary skill, when applying Beaverton's apparatus and method, <u>would not be directed to erasing the entire initialization program as the Applicants teach and claim.</u>"** File History, Feb. 23, 2000 Amendment, p.3-4, remarks re independent claims 1, 6 and 22 [issued 18].
4. said memory being of a type, which is	18(b) 19, 20,	Rembrandt does not believe this term requires construction. In the alternative: nonvolatile memory	the system enables all contents in the system's non-volatile memory to be erased and overwritten during

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completely updatable in its entirety but non-volatile	21	which may be overwritten. Intrinsic Support: See support cited for construction of said memory being of a type which may be completely updated in its entirety but which is not volatile	an update Intrinsic Support: FIGS. 1-3. "In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded." Abstract. "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:3-5. "Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where

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			the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled"." 1:6-10. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. **"In accordance with the principles of this invention, the <u>entire set of programs</u> contained in memory 20 can be <u>over-written</u> with a new set of programs…"** 3:47-49. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20

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			halves." 4:21-27. **"To summarize the downloading process of this invention,** **1. Bulk erase … that half of memory 20 which does NOT contain the EP set of programs; …** **4. Bulk erase the other half of memory 20[.]"** 4:28-35. **"1. Bulk erase the second half of memory 20; …** **5. bulk erase the first half of memory 20[.]."** 4:49-55. "In particular, by storing all programs, including the initialization program, in EEPROM, and by providing a means by which two events can occur -- namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs -- it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a non-writeable (ROM)

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			device." File History, Sept. 30, 1997 Amendment, p. 3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized." File History, Sept. 30, 1997 Amendment, p. 5. "The present invention provides a unique approach to solving a problem which is present in a number of microprocessor based devices, i.e., the inability to upgrade all the firmware of the device in the field…. In particular, by storing all programs, including the initialization program, in EEPROM which can be written to by the user, and by providing a means by which two events can occur – namely, the partial erasing of the EEPROM, to provide space for a new initialization program and a subset of the main programs, followed by the memory remapping of the initialization program and main programs – it is possible to provide a modem (or other computer hardware) which can be upgraded in the field, with the

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U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			upgrade being made to all programs including the initialization program, all without requiring storage of any program information (including any initialization program information) in a nonwriteable memory. As will be illustrated below, unlike the present invention, *Beaverton* requires the storage of certain program information in a nonwriteable memory and is, therefore, clearly distinguishable from the present invention. The present invention, as defined by independent claims 1, 6, 8, 13 [issued 10] and 22 [issued 18], includes a memory which is required to be non-volatile and <u>capable of being updated</u>." [applicant's underscore] File History, Jan. 20, 1998 Amendment, pp.3-4, remarks re all independent claims. "Like the present invention, *Beaverton* teaches a system in which all of the memory is EEPROM. However, in contrast to the present invention, *Beaverton* specifically "provides for the firmware resident in the EEPROM to be hardware partitioned into protected and unprotected areas. **The partitioning of the firmware prevents a user from writing over selected partitions of the firmware resident in the EEPROM.** This insures that a

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			minimum amount of firmware is constant in the system . . ." (*Beaverton*, col. 2, lines 51-57) (emphasis added [by applicant]). "The invention [in *Beaverton*] provides a control logic device to maintain a preselected amount of firmware in a protected partition <u>to prevent overwriting **by the user** . . .</u>" (*Beaverton*, col. 3, lines 30-33) (emphasis added [by applicant]). The EEPROM memory in *Beaverton* is partitioned into three ranges, a writeable range, a conditionally rewriteable range, and a protected (nonwriteable) range. (*Beaverton*, col. 5, lines 16-68; col. 6, lines 1-14; FIGS. 3 and 4). "The lower address range (20040000 to [20041FFF]) partition 37 is a nonwriteable partition reserved for the firmware entry code <u>that can never be written to **by a user**</u>." (*Beaverton*, col. 5, lines 67-68; col. 6, lines 1-2) (emphasis added [applicant's underscore]). This limitation makes clear that *Beaverton* does not contain al the elements of the present invention in that ***Beaverton's* partitioned and partially protected (i.e., nonwriteable) "memory" is not the same element as the "memory" of the present invention, which is capable of being updated.** By prohibiting the user from writing over certain portions of the firmware, *Beaverton* clearly did not consider the

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			possibility of the present invention, **namely the ability of a user to update <u>all</u> of the firmware in the system *by overwriting* the memory containing such firmware. [applicant's underscore]** To summarize, the concept of the present invention, namely to be able to change all the programs in the system, including the initialization programs, was not mentioned in *Beaverton* and, in fact, is specifically prohibited by *Beaverton*. The inventors in *Beaverton* knew of (and used) non-volatile EEPROMs as their system memory, but required partitioning of the memory and storage of their firmware entry code in a nonwriteable portion of the EEPROM. This clearly shows that their invention does not anticipate **the use of a memory which can be completely overwritten** so that **all** the programs in the system, including the system initialization programs, can be updated by writing new programs into the memory. **By prohibiting the user from writing to certain portions of its system memory, *Beaverton*, in fact, teaches away from the present invention.** " File History, Jan. 20, 1998 Amendment, pp.5-6, remarks independent claims 1, 6, 8 and 22 [issued 18]. "Both *Beaverton* and *Ahlin* teach a system having a

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			memory that has a non-writeable portion. There is nothing in those patents that can be combined to remove the limitation that a portion of the memory must be non-writeable. **Likewise, neither *Beaverton* nor *Ahlin*, alone or in combination, teach a system having a memory that is capable of being fully updated**, including the updating of the system initialization programs, through a communications port." File History, Jan. 20, 1998 Amendment, p. 9. "(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a [single] type which may be <u>completely</u> updated <u>in its entirety</u> but which is not volatile, said memory being the only program memory in said system" (Note that this amendment was submitted because the applicant's 1/2/98 Remarks alone were considered insufficient) File History, Apr. 2, 1998 Amendment, p.2, re claim 1. "Applicants believe that Beaverton teaches a system for updating programs stored in an EEPROM by storing a new sub-routine into a new location on an EEPROM, and then updating a second transfer vector identifying the starting address of the new subroutine.

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			However, in Beaverton, at least one program portion resides in a *protected* partition within the EEPROM and other program portions reside in an unprotected partition within the EEPROM. Program software in Beaverton can only be loaded onto the *unprotected* partition of the EEPROM (column 3, lines 1-9). Beaverton provides that the protected partition of the EEPROM is a "non-writable partition reserve for the firmware entry code that can never be written to by a user." (See column 5, line 67 to column 6, line 2.) [applicant's emphasis] In contrast, the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications … are downloadable. That is, the apparatus of employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only memory" (page 3, lines 9-13). Applicants, therefore, respectfully submit that there are no teachings in Kreifels (which Applicants believe to merely teach an apparatus and method for the writing to and the erasing of an EEPROM memory device) to combine with the teachings of Beaverton (which Applicants believe to teach program software

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			residing in an EEPROM with **a portion of the software residing in a protected, non-writeable partition) t**o arrive at the Applicants' present invention, which teaches at least the elements of an initialization program residing in a memory in which the initialization program may be completely updated in its entirety. More specifically, claim 1 recites the limitation of "a memory being of a type which may be completely updated in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Claim 6 recites the limitation of a "memory being completely updatable in its entirety" and "a set of programs stored in said memory that are executed when the system needs to be initialized." Furthermore, claim 22 recites the limitation of a "memory being of a type which is completely updatable in its entirety" and "a set of program means stored in said memory that are activated when said system needs to be updated." … In addition, a reference "teaches away" from the claimed invention and should not be used to reject the claimed invention under §103 "when a person of ordinary skill, upon reading the reference, would be

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			discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." … **Applicants believe that one of the critical inventive steps in Beaverton is that a non-writable partition provides security for the initialization program. Therefore, Applicants submit that a person of ordinary skill, when applying Beaverton's apparatus and method, <u>would not be directed to erasing the entire initialization program as the Applicants teach and claim.</u>**" File History, Feb. 23, 2000 Amendment, p.3-4, remarks re independent claims 1, 6 and 22 [issued 18].
5. memory . . . not volatile memory . . . non-volatile	1(b), 2, 3, 4, 5, 6(b), 7, 8(b), 10(c), 11, 12, 13, 14, 15, 16, 17, 18(b), 19, 20, 21	Rembrandt does not believe this term requires construction. In the alternative: memory that retains its contents when power to the memory is disconnected. Intrinsic Support: "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. Col. 4, 15-18. This set of	memory that retains its contents when power to the memory is disconnected Intrinsic Support: "This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss." 1:57-58. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile."

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		programs should, of course, be a non-volatile store because there is always a possibility of power loss."1:58; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31..	4:35-37.
<u>6.</u> said memory being the only program memory in said [the] system	1(b), 2, 3, 4, 5, 6(b), 7	Rembrandt does not believe this term requires construction. In the alternative: the only memory used by the system for non-volatile storage of initialization programs. <u>Intrinsic Support:</u> See definition of "program memory".	the system's completely updateable nonvolatile memory is the only memory from which the system executes programs <u>Intrinsic Support:</u> FIGS. 1-3. "The problem of downloading a modified version of the <u>operating communication program</u>, and the problem of effectively updating the <u>entire set of programs</u> in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. "All programs (including the boot-up programs) can be stored in a <u>single memory arrangement</u> which, for some applications, can consist of just two memory

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			blocks." 2:44-46. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14 respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20." 2:47-58. "A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67.

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			"It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that <u>memory 20 must be non-volatile.</u>" 4:15-17. "The operation of the FIG. 1 apparatus is quite simple. <u>The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20</u> via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. "<u>The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20</u>, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:40-44. "In accordance with the principles of this invention, <u>the entire set of programs contained in memory 20</u> can

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			be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, <u>a command is received on line 12 to branch to the subroutine in the EP set</u> that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:47-56. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, <u>because two EP sets must temporarily coexist in memory 20.</u> After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. <u>The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set.</u> That means that the program in the new EP set

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			to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-17. "2. download a new EP set of programs to the erased half of memory 20; … 5. download the remainder of programs into memory 20." 4:30-36. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not

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			the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves." 4:21-27. "2. download a new EP set of programs to the second half of memory 20; … 8. download the remainder of programs into memory 20." 4:50-59. "The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped." File History, Apr. 26, 1996 Amendment, p. 4. "With respect to Claim 3, Mori uses **_both_** ROM memory 30 **_and_** memory 20, so **_neither_** can be '**_the only program memory in the system_**', as required by Claim 3." File History, Sept. 16, 1996 Amendment, p.4 (emphasis in original). "In the present invention, the initialization program is located in the single memory, which is a non-volatile EEPROM." File History, Mar. 10, 1997 Amendment, p. 7-8. "The present invention, as defined by independent

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			claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (See Col. 4, lines 63-68). In the present invention, the initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the system. In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still

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				operating." File History, Sept. 30, 1997 Amendment, p. 8. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
7.	program memory	1, 6	Updateable and non-volatile memory where initialization programs are stored. Intrinsic Support:	the system's completely updateable nonvolatile memory is the only memory from which the system executes programs Intrinsic Support:

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		"[M]emory,…programs stored in said memory that are executed when the system needs to be initialized…." Claim 1, '159 patent. "The operation of the FIG.1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11…The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses 'virtual addresses', which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30…This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous	FIGS. 1-3. "The problem of downloading a modified version of the <u>operating communication program</u>, and the problem of effectively updating the e<u>ntire set of programs</u> in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." 1:66-2:4. "All programs (including the boot-up programs) can be stored in a <u>single memory arrangement</u> which, for some applications, can consist of just two memory blocks." 2:44-46. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14 respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In

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		segment of memory 20 addresses in the range 0 to N." 3:16-44. "Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories…That resident portion contains 'boot-up' segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the 'essential programs' (EP) set…." 1:51-2:4. "…In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only-memory…." 2:29-44. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory." 2:47-49.	FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20." 2:47-58. "A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-17. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by

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		"The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending out information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:31-39. "In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:1-5. FIGS. 1-3. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:40-44. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:47-56. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily

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			coexist in memory 20.
			After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.
			The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14.

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			"It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that <u>memory 20 must be non-volatile."</u> 4:15-17. "2. download a new EP set of programs to the erased half of memory 20; … 5. download the remainder of programs into memory 20." 4:30-36. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves." 4:21-27. "2. download a new EP set of programs to the second half of memory 20; … 8. download the remainder of programs into memory 20." 4:50-59. "The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped." File History, Apr. 26, 1996 Amendment,

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			p. 4. "With respect to Claim 3, Mori uses **_both_** ROM memory 30 **_and_** memory 20, so **_neither_** can be '**_the only program memory in the system_**', as required by Claim 3." File History, Sept. 16, 1996 Amendment, p.4 (emphasis in original). "In the present invention, the initialization program is located in the single memory, which is a non-volatile EEPROM." File History, Mar. 10, 1997 Amendment, p. 7-8. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (See Col. 4, lines 63-68). In the present invention, the

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			initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be <u>divided into sections, so that one of the sections could be erased while the other section was in active use</u>, thereby changing the IPL while the system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the system. In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still operating." File History, Sept. 30, 1997 Amendment, p. 8. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office

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			Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
8. a set of programs stored in said memory that are executed when the system needs to be initialized	1, 2, 3, 4, 5, 6, 7	Rembrandt does not believe this term requires construction. In the alternative: the set of programs used by the system to initialize it. Intrinsic Support: "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the	the set of programs used by the system to initialize it, including the boot up program for the apparatus and programs needed to maintain communications between the apparatus and a remote processor, that are stored in and executed from nonvolatile memory when the system is powered on or re-booted Intrinsic Support: FIGS. 1-3 "**The fact that the EP set is needed to maintain communications** presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication." 1:59-63:

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		party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:47-51. "In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only memory." 2:39-43. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31. FIGS. 1-3.	"In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set." 1:49-56. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package." 2:9-19. "These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs--including the EP set of

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			programs that carry out the elemental communications--are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory blocks. " 2:38-46. "A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable."2:29-41.

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			"A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67. "The operation of the FIG. 1 apparatus is quite simple. <u>The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20</u> via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. "<u>The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20</u>, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a

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			new EP set." 3:40-46. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:47-56. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

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			The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14.
			"It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-17.
			"1. (Thrice Amended) A system [containing] comprising; (a) a processor[,]; (b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, [the improvement comprising:] said memory being of a single type which may be updated but which is not

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			volatile, said memory being the only program memory in said system and (c) alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing." File History, Mar. 10, 1997 Amendment, p. 2. "6. (Thrice Amended) A system [containing] comprising; (a) a processor[,]; (b) a memory coupled to [the] said processor memory, said memory being of a single type and which is the only program memory in the system, said memory being updatable but non-volatile, [and] there being a set of programs stored in said memory that are executed when the system needs to be initialized[, the improvement comprising:]; and (c) alterable memory means for storing a multi-bit memory address that controls the starting address accessed by the processor when initializing." File History, Mar. 10, 1997 Amendment, p. 2. 3/10/97 Remarks re rejection of claims 2, 4 [issued 3], 23 [issued 19] and 25 [issued 20]: "Both [Lang and Hirano] taught the use of EEPROMs, but neither one taught or suggested the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which

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			enabled switching in a new initialization program together with a memory remapping, whereby **new initialization programs** could be entered into the **boot memory**. … Neither patent suggests or teaches the ability to provide a new downloaded initialization program which can be activated by memory remapping. … In the present invention, on the other hand, the **initialization programs**, **including the communications programs** can be changed while the system is still operating. 3/10/97 Remarks re rejection of claims 2, 4, 23 and 25: "Even if Hirano et al. were [led] to use an EEPROM, rather than a ROM as their initialization program loader, based upon Lang's teachings, in following Lang's teachings they would have been lead away from the use of memory remapping. **Further, there is no teaching in Lang or in Hirano et al. that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate.**" "In particular, by storing all programs, including the initialization program, in EEPROM, … " File History,

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			Sept. 30, 1997 Amendment, p. 3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (*See* Col. 4, lines 63-68). In the present invention, the initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the

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			system. <u>In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still operating.</u> . . . For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." File History, Sept. 30, 1997 Amendment, p. 8. 2/23/00 Response re claims 1, 6 and 22 [issued 18].: "Applicants respectfully submit that Kreifels fails to teach or suggest anything regarding the content of the memory in the EEPROM, such as essential portion (EP) sets, BIOS codes, addresses or effectors. Since the Applicants' present invention does not teach or claim any aspect of the process, method or apparatus for erasing an EEPROM or writing to an EEPROM, the Applicants believe that the teachings of Kreifels do not suggest any features of the Applicants' claimed invention…. In contrast, **the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications** … are downloadable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98

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			Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
9.	said memory containing programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication	10(c), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: a program that, when executed, provides communication with remote devices via the communication port. Intrinsic Support: "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with	the set of programs used by the system to initialize it, including the boot up program for the apparatus and programs needed to maintain communications between the apparatus and a remote processor, that are stored in and executed from nonvolatile memory when the system is powered on or re-booted Intrinsic Support: FIGS. 1-3

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through said communication port		a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively." 2:47-54; "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. 3:40-45; FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	"**The fact that the EP set is needed to maintain communications** presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication." 1:59-63 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set." 1:49-56. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded

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			EP set of the new communication package, the second segment downloads the remainder of the new package." 2:9-19. "These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory blocks. " 2:38-46. "A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by

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			the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs-- including the EP set of programs that carry out the elemental communications--are downloadable."2:29-41.

"A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67.

"The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. |

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			"The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:40-46.

"In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:47-56.

"In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations |

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile."

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			4:15-17. "1. (Thrice Amended) A system [containing] comprising; (a) a processor[,]; (b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, [the improvement comprising:] <u>said memory being of a single type which may be updated but which is not volatile, said memory being the only program memory in said system and</u> (c) alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing." File History, Mar. 10, 1997 Amendment, p. 2. "6. (Thrice Amended) A system [containing] comprising; (a) a processor[,]; (b) a memory coupled to [the] said processor memory, said memory being of a single type and which is the only program memory in the system, said memory being updatable but non-volatile, [and] there being a set of programs stored in said memory that are executed when the system needs to be initialized[, the improvement comprising:]; and (c) alterable memory means for storing a multi-bit memory address that controls the starting address accessed by the processor when initializing." File

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			History, Mar. 10, 1997 Amendment, p. 2. "In particular, by storing all programs, including the initialization program, in EEPROM, … " File History, Sept. 30, 1997 Amendment, p. 3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (*See* Col. 4, lines 63-68). In the present invention, the initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section

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			was in active use, thereby changing the IPL while the system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the system. <u>In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still operating.</u> . . . For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." File History, Sept. 30, 1997 Amendment, p. 8. 2/9/95 Remarks: "New claims 12-26 are added to more fully define the invention. The notion of modifying a program through a transmission from a communication port is not described by the [Lang] reference (the connection between a disk drive and the computer's processor is not considered a communication port) **and the notion of modifying a program that relates to the transmission through the communication port while the communication port is in use** is certainly not described or suggested by the reference." 4/26/96 Remarks: "With respect to claim 13 [issued 10], the Examiner argued that claim 13 was considered to consist of a processor, a port, a memory,

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			and means for receiving information. As such, the Examiner contended that these means are taught by the system of Lang. … Here the Examiner is wrong, because Claim 13 also includes, ". . .means for activating said program for controlling communication and receiving information through the communication port to modify programs in said memory, said information including **the program for controlling communication** through said communication port and a command that is executed by the processor effectively when it is received." **The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped.** Lang does not teach that. In fact, Lang specifically teaches placing parts of the **initial program loader and the basic input-output system** (BIOS) in *unswitched* memory M. (See Col. 3, lines 19-24)." 3/10/97 Remarks re rejection of claims 2, 4, 23 and 25: "Even if Hirano et al. were [led] to use an EEPROM, rather than a ROM as their initialization program loader, based upon Lang's teachings, in following Lang's teachings they would have been lead away from the use of memory remapping. **Further, there is no teaching in Lang or in Hirano et al. that**

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			the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate." 9/30/97 Amendment : "In light of the amendment to Claim 13 [now claim 10], Applicants respectfully contend that the combination of *Hirano* and *Ahlin* would fail to teach one of ordinary skill in the art how to make Applicants' invention. There is simply no teaching in either reference as to the **updating of the initialization programs** through a communication port. … . In contrast, in the system defined in amended claim 13 of the present application, the initialization programs are stored in a non-volatile but writeable memory, which is capable of being updated through the communication port. Accordingly, neither *Hirano* nor *Ahlin*, alone or in combination, **teach the updating of system initialization programs through a communication port."** *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92

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			Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
10. a program module in said memory that, when activated by said processor, effects communication with said port	8(c), 9	Rembrandt does not believe this term requires construction. In the alternative: a set of instructions that, when executed by the processor, provides communication with remote devices via the communication port. Intrinsic Support: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4,	the set of programs that upon execution by the processor from the system's non-volatile memory, enable the system to boot-up and communicate with a remote processor through the communications port Intrinsic Support: FIGS. 1-3 "**The fact that the EP set is needed to maintain communications** presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support

U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
		"The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.)". 3:16-23. Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): See support cited for "communications port". FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	communication." 1:59-63 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. <u>That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set.</u> This set of programs should, of course, be a <u>non-volatile store</u> because there is always a possibility of power loss. The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication." 1:49-63. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address

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			specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package." 2:9-19. "A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs-- including the EP set of programs that carry out the elemental communications--are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist

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			of just two memory blocks. ""2:29-46. "The operation of the FIG. 1 apparatus is quite simple. <u>The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11.</u> In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. "A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67. "<u>The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20,</u> but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a

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			new EP set." 3:40-46. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:47-56. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

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			The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-17. "Amended claim 8 addresses itself to a system that includes a communication program module." File History, Sept. 21, 1995 Amendment, p.7.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			"The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped." File History, Apr. 26, 1996 Amendment, p. 4. "8. (Thrice Amended) A system [containing] comprising; (a) a processor[,]; (b) a memory [coupled to the processor] and a communications port coupled to [the] said processor, said communications port being adapted to communicate with devices which are external to said system, said memory being of a single type and being updatable but non-volatile [the improvement comprising:]; (c) a program module in said memory that, when activated by said processor, effects communication with said port[,]; and (d) operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port." File History, Mar. 10, 1997 Amendment, p.3. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of

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			programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (*See* Col. 4, lines 63-68). In the present invention, the initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the system. In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still operating. . . . For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." File History, Sept. 30, 1997 Amendment, p. 8.

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			2/9/95 Remarks: "New claims 12-26 are added to more fully define the invention. The notion of modifying a program through a transmission from a communication port is not described by the [Lang] reference (the connection between a disk drive and the computer's processor is not considered a communication port) **and the notion of modifying a program that relates to the transmission through the communication port while the communication port is in use** is certainly not described or suggested by the reference." 4/26/96 Remarks re rejection of independent claims 1, 6, 8, 22 [issued 18]: "Thus, the **boot (initialization)** in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard." 9/16/96 Remarks: "Claim 13 [issued 10] stands rejected under 35 U.S.C. §102 as reading upon Mori. Applicant respectfully contends that the Examiner is

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			incorrect for numerous reasons. First, Mori includes no communication port. Even if Mori had a communication port, **it would be inherently incapable of use for modifying the IPLs**, which Mori stores in a non-writable ROM 30. **In the preferred embodiment of Applicants' invention only two IPLs – the one in use and the "new" one (i.e., the one which was downloaded through the communication port) are retained in the EEPROM,** as there is no limit to how many "new" IPLs can thereafter be downloaded. Mori, on the other hand, provides for four IPLs in the fixed ROM 30, any one of which can be bank selected. **Unlike Applicants' invention**, however, Mori starts with and always has four IPLs to select from in the ROM 30. **If Mori wants to provide a "new" IPL**, then the ROM 30 must be physically replaced. Due to these differences, Applicant respectfully contends that Claim 13 does not read on the device of Mori."3/10/97 Remarks re rejection of claims 2, 4 [issued 3], 23 [issued 19] and 25 [issued 20]: "Both [Lang and Hirano] taught the use of EEPROMs, but neither one taught or suggested the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program

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			together with a memory remapping, whereby **new initialization programs** could be entered into the **boot memory**. … Neither patent suggests or teaches the ability to provide a new downloaded initialization program which can be activated by memory remapping. … In the present invention, on the other hand, the **initialization programs**, **including the communications programs** can be changed while the system is still operating. 3/10/97 Remarks re rejection of claims 2, 4, 23 and 25: "Even if Hirano et al. were [led] to use an EEPROM, rather than a ROM as their initialization program loader, based upon Lang's teachings, in following Lang's teachings they would have been lead away from the use of memory remapping. **Further, there is no teaching in Lang or in Hirano et al. that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate.**" 9/30/97 Remarks re rejection of independent claims 1, 6, 8 and 22 [issued 18], "Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one taught or suggested the unique combination set forth

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			in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby **new initialization programs** could be entered into the **boot memory**. Accordingly, Applicants respectfully submit that there is no suggestion in either Hirano or Lang of the need, desire, or benefits to be derived from using an EEPROM to retain the initialization programs. Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be activated by using memory remapping…. **Further, , there is no teaching in Lang or in Hirano that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate**. … In the present invention, on the other hand, the **initialization programs**, **including the communications programs** can be changed while the system is still operating." 2/23/00 Response re claims 1, 6 and 22 [issued 18].: "Applicants respectfully submit that Kreifels fails to teach or suggest anything regarding the content of the memory in the EEPROM, such as essential portion

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			(EP) sets, BIOS codes, addresses or effectors. Since the Applicants' present invention does not teach or claim any aspect of the process, method or apparatus for erasing an EEPROM or writing to an EEPROM, the Applicants believe that the teachings of Kreifels do not suggest any features of the Applicants' claimed invention…. In contrast, **the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications** … are downloadable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response;

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11. set of program means stored in said memory that are activated when said system needs to be updated with a new set of programs	18(c), 19, 20, 21	Rembrandt does not believe this term requires construction. In the alternative: set of programs stored in the memory that, when executed, support updating the system with a new set of programs. Intrinsic Support: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4, The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.)." 3:16-19,	set of programs used by the system to initialize it, including the boot up program for the apparatus, programs needed to maintain communications between the apparatus and a remote processor, and subroutines for updating the system's programs, that are stored in and executed from nonvolatile memory when the system is powered on or re-booted Intrinsic Support: FIGS 1-3 "**The fact that the EP set is needed to maintain communications** presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication." 1:59-63 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. That resident portion contains "boot-up" segments and program segments that are necessary to

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		"This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write	maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss. The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication." 1:49-63. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package." 2:9-19. "A modem's primary function is to enable

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		memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12." 3:35-56. "In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem." 2:33-36; FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs-- including the EP set of programs that carry out the elemental communications--are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory blocks. ""2:29-46. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory." 2:47-49.

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			"A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 2:61-67. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-7. "In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set." 3:11-13. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives

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			from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the address applied to memory 20 (typically by controlling a 'program counter' within processor 10, which is not shown in the FIG.)." 3:16-23. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:40-46. "In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is

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			also downloaded." 3:52-59. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset

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			present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). " 3:62-4:14. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-17. "Both taught the use of EEPROMs, but neither one taught or suggested the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby new initialization programs could be entered into the boot memory." File History, Mar. 10, 1997 Amendment, p. 13. "22. (Amended) A system comprising: (a) a processor[;] (b) a memory coupled to [the] said processor, said memory being of a single type, said memory being updatable but non-volatile; (c) a set of program means stored in said memory that are activated when [the] said system needs to be updated with a new set of [said] programs, and (d) alterable

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			storage means for holding an offset memory address that is used to point to a starting address accessed by [the] said processor when initializing." File History, Sept. 30, 1997 Amendment, p. 4. "The present invention, as defined by independent claims 1, 6, 8 and 22 (as previously amended), includes a memory which is of a single type which may be updated but which is not volatile and which is the only program memory in the system, and a set of programs stored in the memory that are executed when the system needs to be initialized. The Examiner took the position that the memory 19 of *Hirano* corresponded to the memory of claims 1, 6, 8 and 22. However, *Hirano's* memory 19 is made up of two types of memory, *i.e.*, a read only memory ("ROM") 20 and a volatile RAM memory portion 19 (*See* Col. 4, lines 63-68). In the present invention, the initialization program is located in the single memory, which is nonvolatile EEPROM." File History, Sept. 30, 1997 Amendment, p. 5. "Further, there is no teaching in *Lang* or in *Hirano* that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the

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			system continued to operate. The only way to change the ROM of *Hirano* is to turn off the system, physically replace the ROM, and then restart the system. <u>In the present invention, on the other hand, the initialization programs, including the communications programs</u> can be changed while the system is still operating . . . For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." File History, Sept. 30, 1997 Amendment, p. 8. 4/26/96 Remarks re rejection of independent claims 1, 6, 8, 22 [issued 18]: "Thus, the **boot (initialization)** in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard." 3/10/97 Remarks re rejection of claims 2, 4 [issued 3], 23 [issued 19] and 25 [issued 20]: "Both [Lang and Hirano] taught the use of EEPROMs, but neither one taught or suggested the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which

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			enabled switching in a new initialization program together with a memory remapping, whereby **new initialization programs** could be entered into the **boot memory**. … Neither patent suggests or teaches the ability to provide a new downloaded initialization program which can be activated by memory remapping. … In the present invention, on the other hand, the **initialization programs**, **including the communications programs** can be changed while the system is still operating. 3/10/97 Remarks re rejection of claims 2, 4, 23 and 25: "Even if Hirano et al. were [led] to use an EEPROM, rather than a ROM as their initialization program loader, based upon Lang's teachings, in following Lang's teachings they would have been lead away from the use of memory remapping. **Further, there is no teaching in Lang or in Hirano et al. that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate.**" 9/30/97 Remarks re rejection of independent claims 1, 6, 8 and 22 [issued 18], "Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one

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			taught or suggested the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby **new initialization programs** could be entered into the **boot memory**. Accordingly, Applicants respectfully submit that there is no suggestion in either Hirano or Lang of the need, desire, or benefits to be derived from using an EEPROM to retain the initialization programs. Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be activated by using memory remapping…. **Further, , there is no teaching in Lang or in Hirano that the IPL EEPROM be divided into sections, so that one of the sections could be erased while the other section was in active use, thereby changing the IPL while the system continued to operate**. … In the present invention, on the other hand, the **initialization programs**, **including the communications programs** can be changed while the system is still operating." 2/23/00 Response re claims 1, 6 and 22 [issued 18].: "Applicants respectfully submit that Kreifels fails to teach or suggest anything regarding the content of the

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			memory in the EEPROM, such as essential portion (EP) sets, BIOS codes, addresses or effectors. Since the Applicants' present invention does not teach or claim any aspect of the process, method or apparatus for erasing an EEPROM or writing to an EEPROM, the Applicants believe that the teachings of Kreifels do not suggest any features of the Applicants' claimed invention…. In contrast, **the Applicants' invention at least teaches "all programs ... including the EP set of programs that carry out the elemental communications** … are downloadable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and

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			Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
12. alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing	1(c), 2, 3, 4, 5	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "alterable storage means for holding a displacement multi-bit memory address". Function: holding a displacement multi-bit memory address. Structure: register 40 (col. 2, line 59, col. 4, lines 37-48). Intrinsic Support: "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20...." 3:16-23.	Means plus function element to be construed pursuant to 112, 6. Function – storing an updateable multiple bit address that is added to a memory address supplied by the processor that changes the first nonvolatile memory location accessed by the processor when the system is powered on or re-booted Structure – updateable offset address register 40 connected to processor 10 and modifier circuit 30 Intrinsic Support: FIGS. 1-3 Spec at 2:9-15 (summary of the invention): "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address

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		"The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:23-30. "Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." 3:59-63. "Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where	specification means is loaded with the appropriate new start address." "In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:54-61. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). <u>The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is</u> that the addresses supplied on bus 14 are not the actual

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		M is the size of memory 20." 2:58-61. FIGS. 1-3. "If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10. Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20)." 4:37-48. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After

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			supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can |

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			be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves. To summarize the downloading process of this

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			invention,
			1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs;
			2. download a new EP set of programs to the erased half of memory 20;
			3. download the offset address to pass control to the new EP set of programs;
			4. bulk erase the other half of memory 20;
			5. download the remainder of programs into memory 20.
			If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):
			1. Bulk erase the second half of memory 20;
			2. download a new EP set of programs to the second half of memory 20;
			4. download the offset address to pass control to the new EP set of programs;
			5. bulk erase the first half of memory 20;
			6. copy the contents of the second half of memory 20 into the first half of memory 20;
			7. reset the offset address to 0; and
			8. download the remainder of programs into memory 20.
			Admittedly, during the copy sequence (which may

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			also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve." 3:40-4:67.
			"According to claim 1 this address is an offset address that is used to point to the starting address accessed by the processor when initializing, and according to claim 6 this address controls the starting address accessed by the processor when initializing." File History, Feb. 9, 1995 Amendment, p.6.
			"Amended claim 1 explicitly states that the alterable storage means holds an [sic] 'displacement multi-bit memory address'. Thus, the claim specifies something that is (a) an address, (b) a memory address, (c) a multi-bit memory address, and (c) [sic] a displacement multi-bit memory address. This address 'points to' the starting address accessed by the processor when initializing." File History, Sept. 21, 1995 Amendment, p.7. 4/26/96 Remarks re rejection of independent claims 1, 6, 8, 22 [issued 18]: "Thus, the **boot (initialization)** in Hugard is always initially the same, and it always starts at the

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			same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard."
			"The Applicant must respectfully disagree with the Examiner's interpretation of Mori, as Mori has neither an 'alterable storage means' nor 'a displacement multi-bit memory address which is used to point to the starting address accessed by the processor when initializing', as set forth in Claim 1." File History, Sept. 16, 1996 Amendment, p.2. "Second, the 'starting address' never changes, as Mori does not perform any remapping. Instead, Mori uses the switches 302, 303, and the chip enable ("CE") port of the ROM 30 to select one of the four 512 x 1 banks in the 512 x 4 ROM for use. In effect, Mori is 'plugging in' one of four possible 512 x 1 ROMs into the same location. As the IPLs of Mori are all located at the same memory address, Mori neither provides for, nor needs, any means for changing the starting

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			address of the program … This selection of a desired one of the IPL programs by Mori, is simply a selection, it is not an address change." File History, Sept. 16, 1996 Amendment, p.5. "The Lang system modifies the initialization routines by zeroing on a segment of the memory where the memory is into area B0 and area B1, and based on an internal state variable S=1 or S=0, either area B0 or B1 is accessed for initialization. The area that is not accessed for initialization is the area that is used to load with a new initialization program, when that is desired. Amended claims 1 and 6 address a different aspect of a system's operation, and the defined structure is different from that which is described in the reference. Particularly, claims 1 and 6 call for a means that is a) alterable, and b) holds a memory address. According to claim 1 this address is an offset address that is used to point to the starting address accessed by the processor when initializing, and according to claim 6 this address controls the starting address accessed by the processor when initializing. No such means exists in the Lang patent. The S variable is alterable, but it does not store an address. That leads to the distinct

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U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			disadvantage for the Lang system which is restricted to placing data either in B0 or in B1, where the two blocks reside in the same addresses (col 3, line 5). In contradistinction, the system of claims 1 and 6 can place updated programs in whatever place is desired." File History, Feb. 9, 1995 Amendment, p.6. "In a previous Office action response, applicants pointed out that internal state variables S and I are not an **address** and that the subject claims define an alterable storage means that holds an offset address that is used to point to a starting address accessed by the processor. The Examiner's current response is that 'the internal state variable of Lang can be considered as a one bit address which specifies where to start executing the initialization code.' Applicants respectfully disagree. Both I and S are internal state variables. They can affect an address, but they themselves are not a <u>memory address</u>. Amended claim 1 explicitly states that the alterable storage means holds an [sic] 'displacement multi-bit memory address'. Thus, the claim specifies something that is (a) an <u>address</u>, (b) a <u>memory</u> address, (c) a <u>multi-bit</u> memory address, and (c) [sic] a <u>displacement</u>

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			multi-bit memory address. This address 'points to' the starting address accessed by the processor when initializing. In contradistinction, the Lang state variable is none of the above. Just because it is a one bit of information, does not mean that it can be considered to be an address, or a memory address. At no time it is used, or can be used, as a memory address. To hold otherwise would rob the phrase 'memory address' of its meaning, since most registers in a microprocessor, for example, at one time or another affect the address that is applied to memory. * * * **Claim 22 [patent claim 18] is similar to claim 1, and the above remarks in connection with claim 1 are adopted to claim 22." File History, Sept. 21, 1995 Amendment, pp. 6-8.** "Claims 1-9, 12-13, and 17-26 [patent claim 18 was application claim 22] stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 5,257,380 entitled INITIALIZATION ROUTINE IN AN EEPROM which issued on October 26, 1993 to G.

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			Lang ("lang") in view of the disclosure contained in U.S. Patent No. 5,136,711 entitled SYSTEM FOR MULTIPLE ACCESS HARD DISK PARTITIONING which issued on August 4, 1992 to J.M Hugard, et al. ("Hugard"). * * * The Examiner acknowledged that Lang does not disclose a 'displacement multi-bit memory address' or 'offset memory address' as is claimed, but rather uses an internal state variable I for indicating the starting address of the initialization programs. Consequently, the Examiner argued, " … Hugard teaches the use of a displacement multi-bit memory address (Hugard's 'offset value' in the 'partition table', col. 2, line 65 - col. 3, line 2) *in the same field of endeavor for the purpose of providing an efficient way of installing selectable multiple initializing code segments."* (emphasis added). The Examiner referred to column 2, lines 27-42 of Hugard for support. The Examiner contended that it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the internal state variable technique of Lang with the offset memory address technique of Hugard, because it would provide

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			Lang with a more efficient way of installing selectable multiple initializing code segments. Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two separate storage areas which have 'identical addresses' (See Abstract; Col. 1, lines 29-33; Col. 3, lines 3-6; FIG. 4). <u>Accordingly, Lang teaches memory **substitution**, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory).</u> Hugard teaches how to maintain two mutually distinct and independent disk operating systems on a single hard drive. Lang teaches nothing about hard drives, and Hugard teaches nothing about changing an initialization sequence contained in read only memory. <u>In fact, Hugard's teachings are also based upon there being a single bit (flag) which is in semiconductor memory (just like Lang), as set forth at column 6, lines 18-27.</u> The specific reference which was indicated to be relevant by the Examiner (i.e., Col. 2, line 54-Col.3, line 5), clearly illustrates that the essential programs of Hugard which are located in semiconductor memory, i.e., the BIOS, are not changed. The same 'first BIOS' always starts during

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			the initialization, and it then identifies the boot mode (based upon a flag -- just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is always operative, i.e., the initialization of the processor is always the same. Thus, the boot (initialization) in Hugard is always initially the same, and it always starts at the same place, in the same semiconductor memory. Lang teaches the use of two different semiconductor memories, where the appropriate one is selected by reading a flag, not by memory remapping. <u>Applicants, on the other hand, teach the use of an "… alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.", something not taught by either Lang or by Hugard, or suggested by either.</u>" File History, Apr. 26, 1996 Amendment, pp. 3-4. 9/16/96 Remarks re claims 1, 2, 4-9, 12, 22, 23, 25 and 26: "Applicants respectfully disagree with the Examiner's position. **First of all, Lang teaches nothing about address modification.** An examination of Lang shows that Lang specifically

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			teaches that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29 33; Col. 3, lines 3 6; FIG. 4). **Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping.** As set forth above, Hirano was already familiar with, and used, EEPROMs. Nevertheless, when it came to holding the initialization programs, Hirano specifically taught the use of a ROM which can retain more than one initialization program. Lang, on the other hand, teaches that [IPL] can be replaced, through memory substitution. Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one taught or suggested **the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby new initialization programs could be entered into the boot memory….** Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be **activated by using memory remapping**. * * *

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			For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." 4/26/96 Remarks re rejection of claims: "Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29-33; Col. 3, lines 2-6; FIG. 4). Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory). … The same "first BIOS" always starting during the initialization, and it then identifies the boot mode (based upon a flag – just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is always operative, i.e., the initialization of the processor is always the same. … Thus, the boot (initialization) in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address

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			that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard. … The offset addresses of Hugard, are hard drive offset addresses, and they are not related to the starting address accessed by the processor when initializing. Accordingly, while Applicants, in any event, would argue that Lang cannot be combined with Hugard, as such combination is not suggested by either, such a combination would not yield Applicants' invention, in any event…. Consequently, in view of the above remarks, Applicant respectfully contends that the claims remaining in the application, i.e., claims 1-9, 12-15, and 17-26 are allowable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97

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			Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
13. alterable memory means for storing a multi bit memory address that controls the starting address accessed by the processor when initializing	6(c), 7	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "alterable memory means for storing a multi-bit memory address". Function: storing a multi-bit memory address. Structure: register 40 (col. 2, line 59, col. 4, lines 37-48). Intrinsic Support: "This protocol provides a mechanism for intelligent communication with processor 10, which includes for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication	Means plus function element to be construed pursuant to 112, 6. Function – storing an updateable multiple bit address that is added to a memory address supplied by the processor that changes the first nonvolatile memory location accessed by the processor when the system is powered on or re-booted Structure – updateable offset address register 40 connected to processor 10 and modifier circuit 30 Intrinsic Support: FIGS. 1-3 "In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is

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		with line 12 and for receiving information from line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N…." 3:35-4:14. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20...." 3:16-23. "The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:23-30. "Optionally, an offset address that is the starting	responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:54-61. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set

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		address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." 3:59-63. "Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:58-61. FIGS. 1-3 "If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or	of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP

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		as part of processor 10. Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20)." 4:37-48. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

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			It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves. To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the

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			new EP set of programs;
			4. bulk erase the other half of memory 20;
			5. download the remainder of programs into memory 20.
			If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.
			Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):
			1. Bulk erase the second half of memory 20;

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			2. download a new EP set of programs to the second half of memory 20;
			4. download the offset address to pass control to the new EP set of programs;
			5. bulk erase the first half of memory 20;
			6. copy the contents of the second half of memory 20 into the first half of memory 20;
			7. reset the offset address to 0; and
			8. download the remainder of programs into memory 20.
			Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power

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			reserve." 3:40-4:67. "According to claim 1 this address is an offset address that is used to point to the starting address accessed by the processor when initializing, and according to claim 6 this address controls the starting address accessed by the processor when initializing." File History, Feb. 9, 1995 Amendment, p.6. "Amended claim 1 explicitly states that the alterable storage means holds an [sic] 'displacement multi-bit memory address'. Thus, the claim specifies something that is (a) an address, (b) a memory address, (c) a multi-bit memory address, and (c) [sic] a displacement multi-bit memory address. This address 'points to' the starting address accessed by the processor when initializing." File History, Sept. 21, 1995 Amendment, p.7. "4/26/96 Remarks re rejection of independent claims 1, 6, 8, 22 [issued 18]: "Thus, the **boot (initialization)** in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			starting address accessed by the processor when initializing', something not taught by… Hugard." "The Applicant must respectfully disagree with the Examiner's interpretation of Mori, as Mori has neither an 'alterable storage means' nor 'a displacement multi-bit memory address which is used to point to the starting address accessed by the processor when initializing', as set forth in Claim 1." File History, Sept. 16, 1996 Amendment, p.2. "Second, the 'starting address' never changes, as Mori does not perform any remapping. Instead, Mori uses the switches 302, 303, and the chip enable ("CE") port of the ROM 30 to select one of the four 512 x 1 banks in the 512 x 4 ROM for use. In effect, Mori is 'plugging in' one of four possible 512 x 1 ROMs into the same location. As the IPLs of Mori are all located at the same memory address, Mori neither provides for, nor needs, any means for changing the starting address of the program … This selection of a desired one of the IPL programs by Mori, is simply a selection, it is not an address change." File History, Sept. 16, 1996 Amendment, p.5.

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U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			"Claims 1-9, 12-13, and 17-26 [patent claim 18 was application claim 22] stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 5,257,380 entitled INITIALIZATION ROUTINE IN AN EEPROM which issued on October 26, 1993 to G. Lang ("lang") in view of the disclosure contained in U.S. Patent No. 5,136,711 entitled SYSTEM FOR MULTIPLE ACCESS HARD DISK PARTITIONING which issued on August 4, 1992 to J.M Hugard, et al. ("Hugard"). * * * <u>The Examiner acknowledged that Lang does not disclose a 'displacement multi-bit memory address' or 'offset memory address' as is claimed, but rather uses an internal state variable I for indicating the starting address of the initialization programs.</u> Consequently, the Examiner argued, " … Hugard teaches the use of a displacement multi-bit memory address (Hugard's 'offset value' in the 'partition table', col. 2, line 65 - col. 3, line 2) *in the same field of endeavor for the purpose of providing an efficient way of installing selectable multiple initializing code segments."*

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			(emphasis added). The Examiner referred to column 2, lines 27-42 of Hugard for support. The Examiner contended that it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the internal state variable technique of Lang with the offset memory address technique of Hugard, because it would provide Lang with a more efficient way of installing selectable multiple initializing code segments. Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two separate storage areas which have 'identical addresses' (See Abstract; Col. 1, lines 29-33; Col. 3, lines 3-6; FIG. 4). Accordingly, Lang teaches memory *substitution*, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory). Hugard teaches how to maintain two mutually distinct and independent disk operating systems on a single hard drive. Lang teaches nothing about hard drives, and Hugard teaches nothing about changing an initialization sequence contained in read only memory. In fact, Hugard's teachings are also based upon there being a single bit (flag) which is in

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U.S. Patent No. 6,131,159	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			semiconductor memory (just like Lang), as set forth at column 6, lines 18-27. The specific reference which was indicated to be relevant by the Examiner (i.e., Col. 2, line 54-Col.3, line 5), clearly illustrates that the essential programs of Hugard which are located in semiconductor memory, i.e., the BIOS, are not changed. The same 'first BIOS' always starts during the initialization, and it then identifies the boot mode (based upon a flag -- just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is always operative, i.e., the initialization of the processor is always the same. Thus, the boot (initialization) in Hugard is always initially the same, and it always starts at the same place, in the same semiconductor memory. Lang teaches the use of two different semiconductor memories, where the appropriate one is selected by reading a flag, not by memory remapping. Applicants, on the other hand, teach the use of an "… alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.", something not taught by either Lang or by Hugard, or suggested by either." File History, Apr. 26, 1996

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			Amendment, pp. 3-4. 9/16/96 Remarks re claims 1, 2, 4-9, 12, 22, 23, 25 and 26: "Applicants respectfully disagree with the Examiner's position. **First of all, Lang teaches nothing about address modification.** An examination of Lang shows that Lang specifically teaches that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29 33; Col. 3, lines 3 6; FIG. 4). **Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping.** As set forth above, Hirano was already familiar with, and used, EEPROMs. Nevertheless, when it came to holding the initialization programs, Hirano specifically taught the use of a ROM which can retain more than one initialization program. Lang, on the other hand, teaches that [IPL] can be replaced, through memory substitution. Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one taught or suggested **the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby new initialization programs could be entered into the**

U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** CONSTRUCTION AND INTRINSIC EVIDENCE	**CABLE PARTIES** CONSTRUCTION AND INTRINSIC EVIDENCE
			boot memory…. Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be **activated by using memory remapping**. * * * For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." 4/26/96 Remarks re rejection of claims: "Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29-33; Col. 3, lines 2-6; FIG. 4). Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory). … The same "first BIOS" always starting during the initialization, and it then identifies the boot mode (based upon a flag – just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is

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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			always operative, i.e., the initialization of the processor is always the same. … Thus, the boot (initialization) in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard. … The offset addresses of Hugard, are hard drive offset addresses, and they are not related to the starting address accessed by the processor when initializing. Accordingly, while Applicants, in any event, would argue that Lang cannot be combined with Hugard, as such combination is not suggested by either, such a combination would not yield Applicants' invention, in any event…. Consequently, in view of the above remarks, Applicant respectfully contends that the claims remaining in the application, i.e., claims 1-9, 12-15, and 17-26 are allowable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance.

U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			See also '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
14. alterable storage means for holding an offset memory address that is used to point to a starting address accessed by said processor when initializing	18(d), 19, 20, 21	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: alterable storage means for holding an offset memory address. Function: holding an offset memory address. Structure: Register 40. (col. 2, line 59, col. 4, lines 37-48). Intrinsic Support:	Means plus function element to be construed pursuant to 112, 6. Function – storing an updateable multiple bit address that is added to a memory address supplied by the processor that changes the first memory location accessed by the processor when the system is powered on or rebooted Structure – updateable offset address register **40** connected to and separate from processor **10** and modifier circuit **30**

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30; "Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." 3:59-63;	Intrinsic Support: FIGS 1-3 "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address." 2:9-15. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:1-5; "The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly." 4:4-8, "1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs;	Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:47-61. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set

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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
		4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:28-36, "1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and" 4:49-59; "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data	of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP

U.S. Patent No. 6,131,159	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		supplied by line 12." 3:1-4, "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.)." 3:16-19, "This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing	sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12." 3:35-56. "In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem." 2:33-36;	It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves. To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20;

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20. If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10. Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20;

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			2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20. Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power

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			reserve." 3:40-4:67. "Amended claim 1 explicitly states that the alterable storage means holds an [sic] 'displacement multi-bit memory address'. Thus, the claim specifies something that is (a) an address, (b) a memory address, (c) a multi-bit memory address, and (c) [sic] a displacement multi-bit memory address. This address 'points to' the starting address accessed by the processor when initializing." File History, Sept. 21, 1995 Amendment, p.7. "Applicants, on the other hand, teach the use of an '…alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.', something not taught by either Lang or by Hugard, or suggested by either." File History, Apr. 26, 1996 Amendment, p.4. "The Applicant must respectfully disagree with the Examiner's interpretation of Mori, as Mori has neither an 'alterable storage means' nor 'a displacement multi-bit memory address which is used to point to the starting address accessed by the processor when initializing', as set forth in Claim 1." File History,

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			Sept. 16, 1996 Amendment, p.2. "Second, the 'starting address' never changes, as Mori does not perform any remapping. Instead, Mori uses the switches 302, 303, and the chip enable ("CE") port of the ROM 30 to select one of the four 512 x 1 banks in the 512 x 4 ROM for use. In effect, Mori is 'plugging in' one of four possible 512 x 1 ROMs into the same location. As the IPLs of Mori are all located at the same memory address, Mori neither provides for, nor needs, any means for changing the starting address of the program … This selection of a desired one of the IPL programs by Mori, is simply a selection, it is not an address change." File History, Sept. 16, 1996 Amendment, p.5. "Applicants disagree with the Examiner. First of all, Lang teaches nothing about address modification. An examination [sic] Lang shows that Lang specifically taught that there are two separate storage areas which have 'identical addresses'. … Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping. … Mori also teaches memory substitution and not remapping." File History, Sept. 16, 1996 Amendment, p.7-8.

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			"In a previous Office action response, applicants pointed out that internal state variables S and I are not an **address** and that the subject claims define an alterable storage means that holds an offset address that is used to point to a starting address accessed by the processor. The Examiner's current response is that 'the internal state variable of Lang can be considered as a one bit address which specifies where to start executing the initialization code.' Applicants respectfully disagree. Both I and S are internal state variables. They can affect an address, but they themselves are not a <u>memory address</u>. Amended claim 1 explicitly states that the alterable storage means holds an [sic] 'displacement multi-bit memory address'. Thus, the claim specifies something that is (a) an <u>address</u>, (b) a <u>memory</u> address, (c) a <u>multi-bit</u> memory address, and (c) [sic] a <u>displacement</u> multi-bit memory address. This address 'points to' the starting address accessed by the processor when initializing. In contradistinction, the Lang state variable is none of the above. Just because it is a one bit of information, does not mean that it can be considered to be an address, or a memory address. At no time it is used, or can be used, as a memory

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			address. To hold otherwise would rob the phrase 'memory address' of its meaning, since most registers in a microprocessor, for example, at one time or another affect the address that is applied to memory. * * * Claim 22 [patent claim 18] is similar to claim 1, and the above remarks in connection with claim 1 are adopted to claim 22." File History, Sept. 21, 1995 Amendment, pp. 6-8. "Claims 1-9, 12-13, and 17-26 [patent claim 18 was application claim 22] stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 5,257,380 entitled INITIALIZATION ROUTINE IN AN EEPROM which issued on October 26, 1993 to G. Lang ("lang") in view of the disclosure contained in U.S. Patent No. 5,136,711 entitled SYSTEM FOR MULTIPLE ACCESS HARD DISK PARTITIONING which issued on August 4, 1992 to J.M Hugard, et al. ("Hugard"). * * *

U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** **CONSTRUCTION AND INTRINSIC EVIDENCE**	**CABLE PARTIES** **CONSTRUCTION AND INTRINSIC EVIDENCE**
			The Examiner acknowledged that Lang does not disclose a 'displacement multi-bit memory address' or 'offset memory address' as is claimed, but rather uses an internal state variable I for indicating the starting address of the initialization programs. Consequently, the Examiner argued, " … Hugard teaches the use of a displacement multi-bit memory address (Hugard's 'offset value' in the 'partition table', col. 2, line 65 - col. 3, line 2) *in the same field of endeavor for the purpose of providing an efficient way of installing selectable multiple initializing code segments."* (emphasis added). The Examiner referred to column 2, lines 27-42 of Hugard for support. The Examiner contended that it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the internal state variable technique of Lang with the offset memory address technique of Hugard, because it would provide Lang with a more efficient way of installing selectable multiple initializing code segments. Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two separate storage areas which have 'identical addresses' (See Abstract; Col. 1, lines 29-33;

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			Col. 3, lines 3-6; FIG. 4). Accordingly, Lang teaches memory ***substitution***, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory). Hugard teaches how to maintain two mutually distinct and independent disk operating systems on a single hard drive. Lang teaches nothing about hard drives, and Hugard teaches nothing about changing an initialization sequence contained in read only memory. In fact, Hugard's teachings are also based upon there being a single bit (flag) which is in semiconductor memory (just like Lang), as set forth at column 6, lines 18-27. The specific reference which was indicated to be relevant by the Examiner (i.e., Col. 2, line 54-Col.3, line 5), clearly illustrates that the essential programs of Hugard which are located in semiconductor memory, i.e., the BIOS, are not changed. The same 'first BIOS' always starts during the initialization, and it then identifies the boot mode (based upon a flag -- just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is always operative, i.e., the initialization of the processor is always the same. Thus, the boot (initialization) in Hugard is always

U.S. Patent No. 6,131,159 **Claim Limitation**	**Claims at Issue**	**REMBRANDT** CONSTRUCTION AND INTRINSIC EVIDENCE	**CABLE PARTIES** CONSTRUCTION AND INTRINSIC EVIDENCE
			initially the same, and it always starts at the same place, in the same semiconductor memory. Lang teaches the use of two different semiconductor memories, where the appropriate one is selected by reading a flag, not by memory remapping. <u>Applicants, on the other hand, teach the use of an "… alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.", something not taught by either Lang or by Hugard, or suggested by either.</u>" File History, Apr. 26, 1996 Amendment, pp. 3-4. 9/16/96 Remarks re claims 1, 2, 4-9, 12, 22, 23, 25 and 26: "Applicants respectfully disagree with the Examiner's position. **First of all, Lang teaches nothing about address modification.** An examination of Lang shows that Lang specifically teaches that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29 33; Col. 3, lines 3 6; FIG. 4). **Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping.** As set forth above, Hirano was already familiar with, and used, EEPROMs. Nevertheless, when it came to holding the initialization programs, Hirano specifically taught the

U.S. Patent No. 6,131,159	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			use of a ROM which can retain more than one initialization program. Lang, on the other hand, teaches that [IPL] can be replaced, through memory substitution. Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one taught or suggested **the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby new initialization programs could be entered into the boot memory….** Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be **activated by using memory remapping**. * * * For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." 4/26/96 Remarks re rejection of claims: "Applicants disagree with the Examiner, as Lang teaches nothing about address modification. An examination Lang shows that Lang specifically taught that there are two

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			separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29-33; Col. 3, lines 2-6; FIG. 4). Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping. On the other hand, Hugard teaches nothing about booting from EEPROM (semiconductor memory). … The same "first BIOS" always starting during the initialization, and it then identifies the boot mode (based upon a flag – just like Lang). It then selectively calls a second BIOS, which remaps the hard drive when called. Either way, the first BIOS is always operative, i.e., the initialization of the processor is always the same. … Thus, the boot (initialization) in Hugard is always initially the same, and it always starts at the same place, in the semiconductor memory…. Applicants, on the other hand, teach use of an 'alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing', something not taught by… Hugard. … The offset addresses of Hugard, are hard drive offset addresses, and they are not related to the starting address accessed by the processor when initializing. Accordingly, while Applicants, in any event, would argue that Lang cannot be combined with Hugard, as such combination is not suggested by

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			either, such a combination would not yield Applicants' invention, in any event…. Consequently, in view of the above remarks, Applicant respectfully contends that the claims remaining in the application, i.e., claims 1-9, 12-15, and 17-26 are allowable." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
15. means for receiving a trigger signal at a telecommunication	7	Means plus function claim language to be construed pursuant to 112, ¶ 6. <u>Means plus function term</u>: "means for receiving a	Means plus function element to be construed pursuant to 112, 6. <u>Function</u> – receiving from a port that communicates

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s input port of the system to begin execution of said programs		trigger signal" Function: Receiving a trigger signal. Structure: Processor 10 programmed to perform the step of monitoring data supplied to the telecommunications port. (Figs. 1 and 2, Col. 3 lines 1-4, 52-56). Intrinsic Support: FIGS. 1 and 2. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:-1-4. "This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:35-39.	with a remote processor a signal to begin executing from the non-volatile memory the set of programs that needs to be executed when the system is powered on or rebooted Structure – processor **10** with port coupled to external communications line **12**, buses **13**, **14**, and **16**, register **40**, modifier circuit **30**, nonvolatile memory **20** containing EP set of programs, and an algorithm implementing steps in Figure 2 or 3 out of nonvolatile memory **20** NOTE: By way of example and without limitation, AOP note that regarding claims 7, 8(d), and 10(d), there is no structure clearly linked to the claimed function, rendering the claims invalid. AOP have set forth the only potentially corresponding structure. Intrinsic Support: FIGS. 1-3 "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with

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		"In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location)." 3:52-56; "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:33-36; '159 Patent File History, Papers 1, 2, 4, 15-18, 21,	a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively." 2:47-54. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-8. "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received

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		24-26, 29, 31.	data in memory 20 or elsewhere." 3:32-39. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12." 3:48-61. "The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can

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			be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 4:4-14 "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:27-36.

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			"Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:46-59. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98

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			Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
16. SKIP TO 824 REMOVED		REMOVED -- INTENTIONALLY BLANK	REMOVED -- INTENTIONALLY BLANK

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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
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U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
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17. operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port	8(d), 9	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "operationally alterable means for setting the starting address" Function: Setting the starting address of program that effects communication with communication port. Structure: register 40 (col. 2, line 59, col. 4, lines 37-48). Intrinsic Support: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution"	Means plus function element to be construed pursuant to 112, 6. Function – while the program module in said memory is operating, downloading and storing an offset address that is added to a memory address supplied by the processor that changes the first memory location accessed by the processor when the system is powered on or rebooted Structure – processor **10** with port coupled to external communications line **12**, buses **11**, **13**, **14**, **15** and **16**, offset address register **40**, modifier circuit **30**, nonvolatile memory **20** containing EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory **20**

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		capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4, The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30, "Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded." 3:57-63.	Intrinsic Support: FIGS 1-3 "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:47-61. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which

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		"The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly." 4:4-8, "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20. If register 40 is to contain the offset address for a substantial time after downloading is accomplished,	are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-8. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30.

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		then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10. Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20;	"The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:32-39. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2,

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		7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:28-59. "In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:1-5. "In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable." 2:40-41, "Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:59; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed

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			EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:40-4:14. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20;

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			5. download the remainder of programs into memory 20." 4:28-36. "If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10." 4:37-44. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs;

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			5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:46-59. "Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve." 4:60-67. Spec at 2:9-15 (Summary of the Invention): "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of

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			programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address." "Also, the communication port must be capable of modifying the programs in the memory, including the program for controlling communication through the communication port." File History, Mar. 10, 1997 Amendment, p. 10. "In the present invention, on the other hand, the initialization programs, including the communications programs can be changed while the system is still operating." File History, Mar. 10, 1997 Amendment, p. 16. 2/9/95 Remarks: "**Claim 8** addresses a slightly different aspect of applicants' invention. **It defines a means that sets the starting position (i.e., address) of a program executed by the system when it is interacting with a communication port, and this setting is pursuant to information supplied to said system via said communication port.** Clearly this aspect is not present in the Lang reference. Since Lang's starting position is known *a priori*, **there is no**

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			need to receive information from a communication port to specify a starting address." 9/16/96 Remarks re claims 1, 2, 4-9, 12, 22, 23, 25 and 26: "Applicants respectfully disagree with the Examiner's position. **First of all, Lang teaches nothing about address modification.** An examination of Lang shows that Lang specifically teaches that there are two separate storage areas which have "identical addresses" (See Abstract; Col. 1, lines 29 33; Col. 3, lines 3 6; FIG. 4). **Accordingly, Lang teaches memory substitution, as indicated by a selectively set bit, not remapping.** As set forth above, Hirano was already familiar with, and used, EEPROMs. Nevertheless, when it came to holding the initialization programs, Hirano specifically taught the use of a ROM which can retain more than one initialization program. Lang, on the other hand, teaches that [IPL] can be replaced, through memory substitution. Therefore, while both Hirano and Lang taught the use of EEPROMs, neither one taught or suggested **the unique combination set forth in the present invention of using EEPROMs to hold the initialization programs, and a means which enabled switching in a new initialization program together with a memory remapping, whereby new**

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			initialization programs could be entered into the boot memory…. Neither patent suggests nor teaches the ability to provide a new downloaded initialization program which can be **activated by using memory remapping**. * * * For the foregoing reasons, Applicants respectfully contend that independent claims 1, 6, 8 and 22 are allowable." 9/21/95 Remarks: "**Amended claim 8** addresses itself to a system that includes **a communication program module. The claim refers to an "operationally alterable means" for setting the starting address of this communication program, and that starting address is supplied via the communication port.** The Lang reference does not have **an address in the alterable means**, and the information that constitutes the internal state variable is not received from the communication port. n paragraph 5(a) of the Office action the Examiner points to claim 7 of Lang, for the proposition that the starting address is changed pursuant to information received via a communication port. Applicants believe that not to be the case. What

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			claim 7 teaches is a process by which information is received and stored in the B storage area that is not is current use. The claim then specifies that a control signal (note that Lang calls the state variable a "control signal") is reset. **Nowhere does Lang say that the value of this control signal is received from the communication port, and nowhere does Lang say, even, that the command to change the value of this control signal, or the trigger for it, comes from the communication port, as specified in amended claim 8.**" 9/16/96 Response: "Further, Claim 8 calls for '. . operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port.' **Thus, inherent in Claim 8 is the ability to receive, via the communication port, a new starting address.** In Mori, that cannot be done for two reasons. Firstly, the "starting address" is not receivable over a communication port, as there is no communication port. **Second, the 'starting address' never changes, as Mori does not perform any remapping.** Instead, Mori uses the switches 302, 303, and the chip enable ("CE") port of the ROM 30 to select one of the four 512 x 1 banks in the 512 x 4 ROM for use. In effect,

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			Mori is 'plugging in' one of four possible 512 x 1 ROMs into *the same location*. As the **IPLs** of Mori are all located *at the same memory address*, Mori neither provides for, nor needs, any **means for changing the starting address** of the program. … This selection of a desired one of the IPL programs by Mori, is simply a selection, **it is not an address change**. Accordingly, Applicant respectfully contends that **Claim 8** does not read on the device described by Mori." [applicant's italics] *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response;

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			5/5/00 Notice of Allowability.
18. means for activating said program for controlling communication	10(d), 11, 12, 13, 14, 15, 16, 17	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for activating said program for controlling communication". Function: Activating program for controlling communication through communication port. Structure: Communication port and processor 10 programmed to perform the step of activating the program for controlling communication. (Figs. 1 and 2, Col. 3 lines 1-4, 16-19, 52-56). Intrinsic Support: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4, ". In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a	Means plus function element to be construed pursuant to 112, 6. Function – activating the program in the nonvolatile memory for controlling communication through said communication port Structure – processor **10** with port coupled to external communications line **12**, buses **11**, **13**, **14**, **15** and **16**, offset register **40**, modifier circuit **30**, nonvolatile memory **20** containing an EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory **20** Intrinsic Support: FIGS 1-3 "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11

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		data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12.: 3:52-56; "Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package. BRIEF DESCRIPTION OF THE DRAWING FIG. 1 presents a block diagram of an arrangement for carrying out this invention; FIG. 2 is a flow diagram of a downloading process in accordance with this invention; and FIG. 3 is a flow diagram of an augmented downloading process in accordance with this invention. DETAILED DESCRIPTION A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a	data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:47-61. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-8. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via

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		transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable." 2:16-41; "This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:35-39; FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30. "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:32-39.

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			"The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset

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			address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of

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			programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:40-4:14. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:28-36. "If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the

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			read/write memory or as part of processor 10." 4:37-44. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:46-59.

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			"Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve." 4:60-67. "Here the Examiner is wrong, because Claim 13 also includes, '…means for activating said program for controlling communication and receiving information through the communication port to modify programs in said memory, said information including the program for controlling communication through said communication port and a command that is executed by the processor effectively when it is received.' The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped." File History, Apr. 26, 1996 Amendment, p.4. *See also* '234 patent file history at 7/24/97

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			Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
19. means for... receiving information through said communication port to modify the programs in said memory, said information including the	10(d), 11, 12, 13, 14, 15, 16, 17	Means plus function claim language to be construed pursuant to 112, ¶ 6. Means plus function term: "means for…receiving information through said communication port". Function: Receiving information through the communication port. Structure: System including memory, communication port, and processor including programmed to perform	Means plus function element to be construed pursuant to 112, 6. Function – receiving in nonvolatile memory through the processor's communication port information which modifies the programs in the system's non-volatile memory, including the activated program for controlling communication in the nonvolatile memory, and a command received directly into the processor and executed

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program for controlling communication through said communication port and a command that is executed by said processor effectively when it is received		the step of receiving information through said communication port to modify the programs in said memory. (Figs. 1 and 2, Col. 3 lines 1-4, 16-19, 52-56). Intrinsic Support: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4, "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11." 3:16-19, "This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside	Structure – processor 10 with port coupled to external communications line 12, buses 13, 14, and 16, offset register 40, modifier circuit 30, nonvolatile memory 20 containing an EP set of programs, and an algorithm for executing either the steps of Figure 2 or 3 out of nonvolatile memory 20 Intrinsic Support: FIGS 1-3 "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is

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		throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12." 3:35-56. "In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle	loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20." 2:47-61. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-8. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual

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		and store the communicated data, as well as the modulation and demodulation programs used by the modem" 2:33-36. FIGS. 1-3; '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31.	addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30." 3:16-30. "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:32-39. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

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			In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are

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			populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:40-4:34. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs;

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			2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:28-36. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20;

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			6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:46-59. "Amended claim 8 addresses itself to a system that includes a communication program module. The claim refers to an 'operationally alterable means' for setting the starting address of this communication program, and that starting address is supplied via the communication port. … Nowhere does Lang say that the value of this control signal is received from the communication port, and nowhere does Lang say, even, that the command to change the value of this control signal, or the trigger for it, comes from the communication port, as specified in amended claim 8." File History, Sept. 21, 1995 Amendment, p.7. "In connection with claim 16, in paragraph 5(d) of the Office action, the Examiner asserts that the limitations are taught by Lang, but that is not the case. … There is no teaching whatsoever to suggest that a command can

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			be injected into the communication port *and that the command is executed when it is received*. That is exactly what amended claim 13 is defining." File History, Sept. 21, 1995 Amendment, p.8 (italics in original). "Here the Examiner is wrong, because Claim 13 also includes, '…means for activating said program for controlling communication and receiving information through the communication port to modify programs in said memory, said information including the program for controlling communication through said communication port and a command that is executed by the processor effectively when it is received.' The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped." File History, Apr. 26, 1996 Amendment, p.4. "Further, as Mori does not disclose 'a communications port coupled to the processor' or 'a program module in said memory that … effects communication with said [communications] port', Claim 8 does not read on the device described by Mori. Further, Claim 8 calls for '…operationally alterable means for setting the starting

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			address of said program, which address is supplied to said system via said communication port.' Thus, inherent in Claim 8 is the ability to receive, via the communication port, a new starting address." File History, Sept. 16, 1996 Amendment, p. 4. "As the purpose of the present invention is to allow for the external updating of the initialization program, it is necessary for the memory of the present invention to be capable of being updated." File History, Mar. 10, 1997 Amendment, p. 8. "Also, the communication port must be capable of modifying the programs in the memory, including the program for controlling communication through the communication port." File History, Mar. 10, 1997 Amendment, p. 10. "As amended herein, the invention defined by Claim 13 includes a communication port and a memory which is non-volatile and capable of being updated, and which contains programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication through the communication port." File

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			History, Sept. 30, 1997 Amendment, p. 9. See 9/21/95 Remarks re claim 13 [issued 10]: "Moreover, the Examiner's explanation appears insufficient inasmuch as the claim explicitly calls for a number of interconnected (structural) elements, and the Examiner appears to simply ignore them. That is, the claim defines a processor, thereafter it defines a communication port coupled to the processor, then it defines a memory coupled to a processor (including a program, and a means for receiving information through the communication port." [applicant's italics] *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment;

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			8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
20. communication[s] port coupled to said processor, said communication port being adapted to communicate with devices which are external to said system	8(b), 9, 10(b), 11, 12, 13, 14, 15, 16, 17	Rembrandt does not believe this term requires construction. In the alternative: an interface through which remote communication is supported, is operatively coupled to a processor to communicate with remote devices. Intrinsic Support: See support cited for "communications port".	communications port connected to the processor so that the processor can receive program data, commands, and other information from remote devices through the port before any such information is stored in any memory Intrinsic Support: FIGS. 1-3 "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively." 2:47-54. "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution"

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			capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." 3:1-8. "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:32-39. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the

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			subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12." 3:48-61. Spec at 1:3-5: "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for **remote updating** of its **entire set** of programs." Spec at 3:1-15: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. **One such normally dormant program is a program that downloads information to the program memory.** It should also be understood, and noted, that although this invention

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			is described in connection with modems, its principles are applicable to all stored program apparatus. In particular, **the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set.** For example, this invention is useful in PCs, "point of sale" terminals, etc." "Amended claim 8 addresses itself to a system that includes a communication program module. The claim refers to an 'operationally alterable means' for setting the starting address of this communication program, and that starting address is supplied via the communication port. … Nowhere does Lang say that the value of this control signal is received from the communication port, and nowhere does Lang say, even, that the command to change the value of this control signal, or the trigger for it, comes from the communication port, as specified in amended claim 8." File History, Sept. 21, 1995 Amendment, p.7. 4/26/96 Remarks: "With respect to claim 13 [issued 10], the Examiner argued that claim 13 was considered to consist of a processor, a port, a memory, and means for receiving information. As such, the Examiner contended that these means are taught by

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			the system of Lang. … Here the Examiner is wrong, because Claim 13 also includes, ". . .means for activating said program for controlling communication and receiving information through the communication port to modify programs in said memory, said information including **the program for controlling communication** through said communication port and a command that is executed by the processor effectively when it is received." **The Examiner has failed to point out any prior art which suggests that the program for controlling communication is also within the memory block being remapped.** Lang does not teach that. In fact, Lang specifically teaches placing parts of the **initial program loader and the basic input-output system** (BIOS) in *unswitched* memory M. (See Col. 3, lines 19-24)." 3/10/97 Remarks: "Claim 13 has been amended to further define the present invention. As amended, Claim 13 requires the presence of a communication port which is adapted to communicate with devices which are external to the system. **Also, the communication port must be capable of modifying the programs in the memory, including the program for controlling communication through the communication port.** *Hirano et al.* describe no

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			such communication port. In particular, while the data bus 9 and terminal 10 of *Hirano et al.* can be used to modify the programs in the **volatile portion** of the memory 19, they cannot modify the programs which control the communication port, for, if they did, it would stop communicating." 1/20/98 Remarks re claim 13 [issued 10]: "Applicants respectfully contend that the combination of *Beaverton* and *Ahlin* would fail to teach one of ordinary skill in the art how to make Applicants' invention. There is simply no teaching in either reference as to the updating of the initialization programs through a communications port. As noted above, *Beaverton* requires that its "firmware entry code" be stored in "a nonwriteable partition" of the system memory "that can never be written to by a user." Thus, it is clear that *Beaverton* specifically prohibits updating of certain portions of the memory, in direct contrast to the present invention. Therefore, *Beaverton* does not disclose the "memory" element of the present invention. … Therefore, it is clear that the initialization programs in *Ahlin* are stored in non-rewriteable ROM and cannot be updated through the communication port. **In contrast, in the system defined in claim 13 of the present application, the**

U.S. Patent No. 6,131,159 Claim Limitation	Claims at Issue	REMBRANDT CONSTRUCTION AND INTRINSIC EVIDENCE	CABLE PARTIES CONSTRUCTION AND INTRINSIC EVIDENCE
			initialization programs are stored in a non-volatile but writeable memory, which is capable of being updated through the communication port. … Both *Beaverton* and *Ahlin* teach a system having a memory that has a non-writeable portion. There is nothing in those patents that can be combined to remove the limitation that a portion of the memory must be non-writeable. Likewise, neither *Beaverton* no *Ahlin*, alone or in combination, teach a system having a memory that is capable of being **fully updated, including the updating of the system initialization programs**, **through a communications port**…. In view of the above remarks, Applicants respectfully submit that independent claim 13, and dependent claims 14-15 and 17-21 are patentable over the cited art." *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action;

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			3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
21. communication[s] port	8, 10, 11, 12, 13, 15, 16, 17	An interface through which remote communication is supported. Intrinsic Support: "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12." 2:47-51; "It should be understood that line 12 in the FIG. 1 architecture effectively offers a 'remote execution' capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12." 3:1-4. "A modem's primary function is to enable	port through which information is downloaded from a remote processor into nonvolatile memory. *See intrinsic support row 20 above. See also* 2:47-55; 2:61-67; 3:6-8; 3:16-19; 3:52-63; 4:10-14; 4:15-17; 4:28-36; 4:49-59.

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		communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem." 2:29-37. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile." 4:15-18. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31. FIGS. 1-3.	

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
<u>1.</u> a memory	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: electronic storage or holding place for data, including instructions. Intrinsic Support: "1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs" Col. 4, lines 45-46. "Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3." Col. 4, lines 62-63 "The operation of the FIG.1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11…The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses	nonvolatile memory Intrinsic Support: FIGS. 1-3 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss." 1:56-65. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start

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		'virtual addresses', which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30…This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere. The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N." 3:25-55. "Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories…That resident portion contains 'boot-up' segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the 'essential programs' (EP) set…." 1:58-2:12.	address specification means and, optionally, with an EEPROM memory." 2:7-12. "All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory devices." 2:53-55. "A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." 3:3-9. "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11." 3:25-28. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"…In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only-memory…." 2:38-52. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory." 2:56-58. "The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending out information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere." 3:41-50. "In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and	communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:51-57. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that <u>memory 20 must be non-volatile.</u>" 4:28-31. "In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." FIG. 1. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action;

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." 5:19-24. FIGS. 1-3. "It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." Col. 4, lines 7-8.	4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
2.	communications programs	1, 5	Programs that support remote communication. Intrinsic Support: "These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable." Col. 2, lines 47-51. "FIG. 3 is a flow diagram of an augmented	The term "communications programs" is used in the context of P_{old} and P_{new} *See rows 4 & 5 below* Intrinsic Support: FIGS. 1-3 "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of

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		downloading process in accordance with this invention" Col 2, lines 33-36 "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:58-63. "In accordance with this invention, all programs— including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile 'boot-up' read-only memory." 2:48-52.	programs." 1:9-11. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory." (2:7-13.) "In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set." 3:20-23. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:58-63. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with

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		'159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31. FIGS. 1-3.	a port for receiving signals from, and sending signals to, line 12." 2:56-60. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
3. communication port	1, 5	An interface through which remote communication is supported. Intrinsic Support: See support cited for the term communication port in	port through which P_{new} programs are downloaded from a remote processor into nonvolatile memory Intrinsic Support: FIGS. 1-3

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		the '159 Claim Construction chart.	"FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively." (2:56-63) "A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing." (3:3-9) "The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the

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			addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.)." (3:25-30) "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." (3:58-4:8)

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			"Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." (4:23-28) "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." (4:44-53) "1. Bulk erase the second half of memory 20;

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			2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." (4:67-5:10) *See also row 5 below* *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action;

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			4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
4.	P_{old}	1, 2, 3, 4, 5, 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: set of communication programs already resident in memory. Intrinsic Support: "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set. In accordance with the principles of this invention, the entire set of programs contained in memory 20	the entire set of programs used by the apparatus, which is stored in and executing from non-volatile memory, when the process to install a new entire set of programs begins Intrinsic Support: "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:9-11. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start

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		can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:58-63. "Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." Col. 4, lines 33-34. Claims 1, 5. Abstract; FIGS. 1-3.	address specification means and, optionally, with an EEPROM memory." 2:7-13. "In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set." 3:20-23. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:58-63. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office

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			Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
5. P_{new}	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a new set of programs to be installed. Intrinsic Support: "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly."	the new entire set of programs (to replace P_{old}), which is stored in and executed from non-volatile memory after downloading into that memory through the communication port from a remote processor Intrinsic Support: FIGS. 1-3 "This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs." 1:9-11. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		Col. 2, lines 9-18. Claim 1, 5. Abstract; FIGS. 1-3.	EEPROM memory." (2:7-13.) "In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set." 3:20-23. "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." 3:58-63. "FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12." 2:56-60. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92

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			Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
6. EP$_{old}$	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a subset of essential programs within P$_{old}$ [defined above] that contains boot-up segments and program segments necessary to maintain communication between the apparatus and a remote device. Intrinsic Support: "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up" segments and program segments that are necessary to	essential subset of the P$_{old}$ set of programs that includes the boot up program for the apparatus and programs needed to maintain communications between the apparatus and a remote processor Intrinsic Support: FIGS. 1-3 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up" segments and program segments that are necessary to

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		maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set." Col. 1, lines 56-63. "This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 4/21-25 Notice of Allowability; pg. 2. Col. 5, lines 34-35; Claims 1, 5. Abstract; FIGS. 1-3. See support for previously defined terms.	maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set." 1:56-63. "The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated." 1:66-2:1. "In accordance with this invention, all programs-- including the EP set of programs that carry out the elemental communications--are downloadable." 2:48-50. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N." 3:51-55. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			See also '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
7. EP$_{new}$	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a subset of essential programs within P$_{new}$ [defined above] that contains boot-up segments and program segments necessary to maintain communication between the apparatus and a remote device. Intrinsic Support: "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains 'boot-up'	essential subset of the P$_{new}$ set of programs that includes the new boot up program and new programs needed to maintain communications between the apparatus and a remote processor Intrinsic Support: FIGS. 1-3 "In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up"

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the 'essential programs' (EP) set." Col. 1, lines 56-63. "This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 4/21-27 Notice of Allowability; pg. 2. Col. 5, lines 34-35; Claims 1, 5. Abstract; FIGS. 1-3. See support cited for previously defined terms.	segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set." 1:56-63. "The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated." 1:66-2:1. "In accordance with this invention, all programs--including the EP set of programs that carry out the elemental communications--are downloadable." 2:48-50. "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N." 3:51-55. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98

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U.S. Patent No. 5,778,234 **Claim Limitation**	Claims at Issue	REMBRANDT **CONSTRUCTION AND INTRINSIC EVIDENCE**	CABLE PARTIES **CONSTRUCTION AND INTRINSIC EVIDENCE**
			Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
8. with the aid of a set of communication programs P_{old} already resident in said memory	1(a), 2, 3, 4, 5(a), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: some of the P_{old} programs [defined above] assist with installing P_{new} programs [defined above]. Intrinsic Support: "A method for installing a new set of communication programs P.sub.new into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs	the P_{old} programs executing from the nonvolatile memory assist with downloading P_{new} programs for use in the nonvolatile memory <u>Intrinsic Support:</u> FIGS. 1-3 "The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated. Indeed, that is

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U.S. Patent No. 5,778,234	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		P.sub.new to said apparatus via said port, with the aid of a set of communications programs P.sub.old already resident in said memory, where said set of programs P.sub.old contains a subset of programs EP.sub.old that occupy less than half of the memory and said set of programs P.sub.new also contains a subset of programs EP.sub.new that, when installed, occupy less than half of the memory, comprising the steps of:" Col. 5, lines 34-35; Claims 1, 5. Abstract; FIGS. 1-3. See support cited for previously defined terms.	often the case with modems, where essentially the sole function of the modem software is to support communication." 1:59-63: "It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory." "The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set." 3:51-57. "In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12." 3:63-4:1.

"The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an |

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of

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			the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M). It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves. 3:50-4:43 *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
9.	installing the EP_{new} programs in a first area of said memory	1(b), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: downloading and storing the EP_{new} programs [defined above] into an area of memory [defined above] that does not contain the EP_{old} programs [defined above]. Intrinsic Support: "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of	downloading and storing EP_{new} programs for immediate execution from a first area of said memory Intrinsic Support: FIGS 1-3 "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated. In accordance with the method of this invention, downloading comprises what may be considered two communication segments." Col. 2, lines 9-18. "To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other)…To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20;	connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." Col. 4, lines 37-53. "It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." 4:15-18. "In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active." Col. 5, lines 19-24. Abstract; FIGS. 1-3. '159 Patent File History, Papers 1, 2, 4, 15-18, 21, 24-26, 29, 31. FIGS. 1-3.	The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:58-4:28. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs;

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			4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:44-53. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
10. said memory	1(b)(d), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: a memory of the apparatus.	memory in which P_{old} is stored and executing Intrinsic Support:

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		Intrinsic Support: See support cited for construction of memory.	FIGS. 1-3 "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:58-4:28. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs;

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			2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:44-53. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response;

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			5/5/00 Notice of Allowability.
11. that contains programs other than the EP_{old} programs, thereby overwriting at least a portion of one program in said P_{old} set of programs	1(b), 2, 3, 4, 5(b), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: EP_{new} [defined above] is installed in an area of memory [defined above] that does not contain EP_{old} programs [defined above] and that includes at least a portion of at least one program in the P_{old} set of programs [defined above]. Intrinsic Support: See support cited for previously defined terms.	installing the EP_{new} programs in a first area of said memory that contains programs other than the EP_{old} programs overwrites at least a portion of one program in said P_{old} set of programs Intrinsic Support: FIGS. 1-3 "In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset

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			address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20. After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of

U.S. Patent No. 5,778,234	Claims at Issue	REMBRANDT	CABLE PARTIES
Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
			programs destined for memory 20 in addresses higher than X+N (modulo M)." 3:58-4:28. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:44-53. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response

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			and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
12. altering operation of said apparatus to execute the EP_{new} programs instead of the EP_{old} programs	1(c), 2, 3, 4, 5(c), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: causing the apparatus to execute EP_{new} programs [defined above] instead of EP_{old} programs [defined above]. Intrinsic Support: "Within that range of addresses there is a subroutine for installing a new EP set " Col. 3, lines 57-59. "Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20." Col. 4, lines 33-34; 53-54.	the apparatus stops executing the EP_{old} programs and immediately begins executing the EP_{new} programs from nonvolatile memory so that communications can continue seamlessly Intrinsic Support: FIGS. 1-3 "A modified version of the operating communication program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment."

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Claim Limitation		**CONSTRUCTION AND INTRINSIC EVIDENCE**	**CONSTRUCTION AND INTRINSIC EVIDENCE**
		"In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2." Col. 3, lines 59-61. "Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20." Col. 4, lines 2-8. Abstract; FIGS. 1-3. See support cited for previously defined terms.	Abstract. "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set." 4:9-23. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response

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			and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
13. installing the remaining programs of said P_{new} set of programs	1(d), 2, 3, 4, 5(e), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: installing the remaining uninstalled programs of the $\underline{P_{new}}$ set of programs [defined above]. Intrinsic Support: "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The	the EP_{new} programs are used to install the remaining programs of the P_{new} set of programs Intrinsic Support: FIGS. 1-3 "A modified version of the operating communication program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the

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		immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. This memory must be erased in bulk before new information can be written in it." Col. 4, lines 12-17, 35-36. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated. In accordance with the method of this invention, downloading comprises what may be considered two communication segments." Col. 2, lines 9-18. Figure 2. Abstract; FIGS. 1-3. See support cited for previously defined terms and for <u>installing the EP_{new} programs in a first area of said memory</u>.	new package of programs is downloaded." Abstract. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package." 2:17-26. "Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 4:23-27. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs;

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			2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:44-53. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20;

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			6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:63-5:10. "1. The following is an examiner's statement of reasons for allowance: The steps of installing the EPnew programs in a first area of memory containing programs other than the EPold programs, thereafter executing the EPnew programs instead of the EPold programs, and installing the remaining programs of the Pnew set of the programs in a second area of memory not occupied by the EPnew programs, as recited in independent claims 10 and 14, are not shown or suggested by the prior art of record. The EPnew programs and the EPold programs in the set of communication programs are defined in the specification, page 2, lines 1-6. It is to be noted that the references considered for the purpose of determining patentability of the claimed subject matter qualify as prior art based on the date of reduction to practice of the invention as established by the

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			Applicants in the Affidavit under 37 CFR 1.131 filed in the parent application (Serial Number 07/880,257 filed May 8, 1992)." File History, Mar. 17, 1998 Notice of Allowance, p.2. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability. *See row 1 above*

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14. remaining programs of said P_{new} set of programs	1(d), 2, 3, 4, 5(e), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: subset of P_{new} programs [defined above] that does not include the EP_{new} programs [defined above]. Intrinsic Support: "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. This memory must be erased in bulk before new information can be written in it." Col. 4, lines 12-17, 35-36. "The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start	subset of P_{new} programs remaining to be transmitted that does not include the previously installed EP_{new} programs Intrinsic Support: FIGS. 1-3 "A modified version of the operating communication program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package of programs is downloaded." Abstract. "In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded

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		address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated. In accordance with the method of this invention, downloading comprises what may be considered two communication segments." Col. 2, lines 9-18. Figure 2. Abstract; FIGS. 1-3. See support cited for previously defined terms and for installing the EP_{new} programs in a first area of said memory.	EP set of the new communication package, the second segment downloads the remainder of the new package." 2:17-26. "Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M)." 4:23-27. "To summarize the downloading process of this invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory

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			20." 4:44-53. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:63-5:10. "1. The following is an examiner's statement of

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			reasons for allowance: The steps of installing the EPnew programs in a first area of memory containing programs other than the EPold programs, thereafter executing the EPnew programs instead of the EPold programs, and installing the remaining programs of the Pnew set of the programs in a second area of memory not occupied by the EPnew programs, as recited in independent claims 10 and 14, are not shown or suggested by the prior art of record. The EPnew programs and the EPold programs in the set of communication programs are defined in the specification, page 2, lines 1-6. It is to be noted that the references considered for the purpose of determining patentability of the claimed subject matter qualify as prior art based on the date of reduction to practice of the invention as established by the Applicants in the Affidavit under 37 CFR 1.131 filed in the parent application (Serial Number 07/880,257 filed May 8, 1992)." File History, Mar. 17, 1998 Notice of Allowance, p.2. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92

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			Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability. *See row 1 above*
15. altering operation of said apparatus to execute said EP_{new} programs is accomplished by installing an offset address to pass control of said apparatus to said EP_{new} programs	4, 8	Rembrandt does not believe this term requires construction. In the alternative: installing an offset address to cause the apparatus to execute the EP_{new} programs [defined above] instead of the EP_{old} programs [defined above]. Intrinsic Support: "Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. Download the remainder of programs into memory 20.	installing an offset address that is added to a memory address supplied by the processor to cause the apparatus to stop executing the EP_{old} programs and immediately begin executing the EP_{new} programs from nonvolatile memory so that communications can continue seamlessly Intrinsic Support: FIGS. 1-3 "A modified version of the operating communication

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		If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20." Col. 4, lines 33-34; 53-54. Abstract; FIGS. 1-3. See support cited for previously defined terms.	program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment." Abstract. "After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address. The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set." 4:9-23. "To summarize the downloading process of this

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			invention, 1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs; 2. download a new EP set of programs to the erased half of memory 20; 3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20." 4:44-53. "Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20;

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			4. download the offset address to pass control to the new EP set of programs; 5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20." 4:63-5:10. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action; 3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment;

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			8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.
16. moving the EP$_{new}$ programs from said first area of memory to a second area of said memory	5(d), 6, 7, 8	Rembrandt does not believe this term requires construction. In the alternative: moving the EP$_{new}$ programs [defined above] into a second area of the memory [defined above]. Intrinsic Support: "3. download the offset address to pass control to the new EP set of programs; 4. bulk erase the other half of memory 20; 5. download the remainder of programs into memory 20. If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10." Col. 4, lines 49-59. Abstract; FIGS. 1-3.	the executing EP$_{new}$ programs move into a second area of the nonvolatile memory Intrinsic Support: FIGS. 1,3 "Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20): 1. Bulk erase the second half of memory 20; 2. download a new EP set of programs to the second half of memory 20; 4. download the offset address to pass control to the new EP set of programs;

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		See support cited for previously defined terms and for installing the EP_{new} programs in a first area of said memory.	5. bulk erase the first half of memory 20; 6. copy the contents of the second half of memory 20 into the first half of memory 20; 7. reset the offset address to 0; and 8. download the remainder of programs into memory 20. Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event." 4:63-5:14. *See also* '234 patent file history at 7/24/97 Amendment #1; 7/24/97 Amendment #2; 3/17/98 Notice of Allowance. *See also* '159 patent file history at 6/25/92 Amendment; 10/6/94 Office Action; 2/9/95 Response and Amendment; 5/10/95 Office Action; 9/21/95 Response and Amendment; 12/12/95 Office Action; 4/26/96 Response and Amendment; 7/31/96 Office Action; 9/16/96 Response; 12/2/96 Office Action;

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			3/10/97 Response and Amendment; 6/9/97 Office Action; 9/30/97 Response and Amendment; 12/30/97 Office Action; 1/20/98 Response; 4/2/99 Amendment; 8/18/99 Office Action; 9/3/99 Amendment and Response; 11/22/99 Office Action; 2/23/00 Response; 5/5/00 Notice of Allowability.